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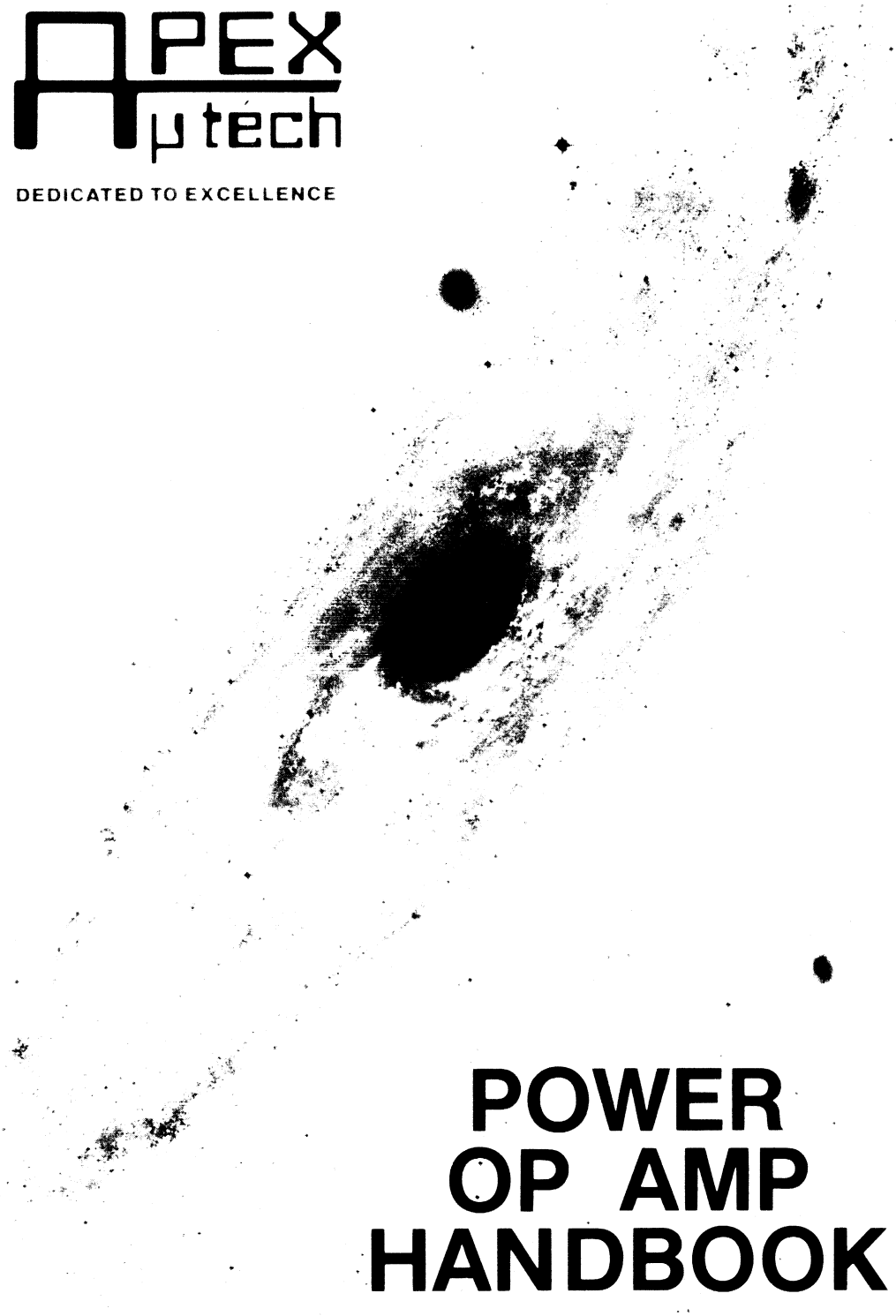
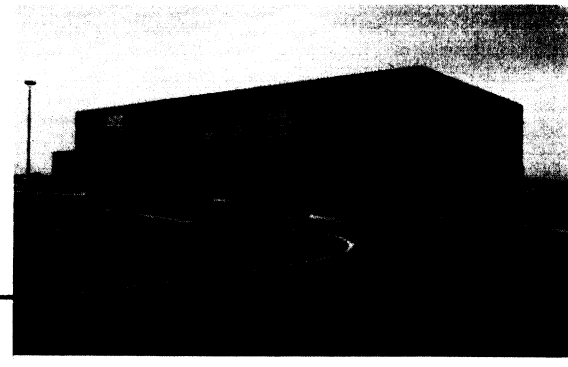


# POWER OP AMP HANDBOOK

*SINCE 1980 . . .*



# WELCOME TO THE INDUSTRY'S MOST INNOVATIVE PRODUCTS . . .

*We thank our customers for their orders which have enabled us to build this company and we will do our best to earn every dollar we receive for our products.*

*In our first 6 years, we have made our customers the number one priority. As a result, marketing has put together the most complete line of Power Op Amps in the industry. Manufacturing produces the highest quality components humanly possible. Engineering is working on the most advanced products imaginable. Sales services you with the fastest off-the-shelf delivery, the largest inventory and the best on-time shipping record in this country. All our employees are dedicated to achieve professional excellence.*

*Should you ever have any problems with any of our staff, my direct line is always open.*

Bill Olschewski

**BILL OLSCHEWSKI**
**PRESIDENT**
**(602) 742-8639**

APEX μ tech

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### APEX MICROTECHNOLOGY CORPORATION LIFE SUPPORT POLICY

As a general policy, APEX MICROTECHNOLOGY CORP does not recommend the use of any of its products in life support applications where the failure or malfunction of the APEX product can be reasonably expected to cause failure of the life support device or to significantly affect its safety or effectiveness. APEX will not knowingly sell its products for use in such applications unless it receives written assurances satisfactory to APEX that the risks of injury or damage have minimized, the customer assumes all such risks, and there is no product liability for APEX.

Examples of devices considered to be life support devices are neonatal oxygen analyzers, nerve stimulators (for any use), autotransfusion devices, blood pumps, defibrillators, arrhythmia detectors and alarms, pacemakers, hemodialysis systems, peritoneal dialysis systems, ventilators of all types, and infusion pumps as well as other devices designated as "critical" by the FDA. The above are representative examples only and are not intended to be conclusive or exclusive of any other life support device.

### APEX LIABILITY IS LIMITED TO REPLACEMENT OF PRODUCT

The APEX product warranty (see page 118) applies only to the original customer and is in lieu of all other warranties, expressed or implied. Under no condition will APEX MICROTECHNOLOGY be liable for any anticipated profits, consequential damages, loss of time or other losses incurred by the customer in connection with the purchase and/or use of the product.

### GENERAL

This catalog has been carefully checked and is believed to be reliable, however, no responsibility is assumed for possible omission or inaccuracies. Specifications are subject to change without notice.

# SELECTOR GUIDE

| Model | Output Current ±A Pk Min | Output Voltage ±V Pk Min | $V_S$-Out Delta V | Supply Range ±V Max | Internal Power Watts Max | $V_{offset}$ Initial mV Max | $V_{offset}$ vs Temp µV/°C Max | I Bias nA Max | $I_q$ mA Max | PWR BW @ Nom $V_{out}$ KHz[2] Typ | Slew Rate V/µs Typ | Unity GBW MHz Typ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA03 | 30 | 68 | 7 | 15/75 | 500 | 3 | 30 | .05 | 300 | 68 | 10 | 5 |
| PA03A | * | * | * | * | * | 1 | 10 | .01 | * | * | * | * |
| PA12A | 15 | 43 | 7 | 10/50 | 125 | 3 | 40 | 20 | 50 | 20 | 4 | 4 |
| PA12M | 10 | 39 | 6 | 10/45 | * | 6 | 65 | 30 | * | * | * | * |
| PA12[4] | * | * | * | * | * | * | * | * | * | * | * | * |
| PA61A[3] | 10 | 39 | 6 | 10/45 | 97 | 3 | 40 | 20 | 10 | 16 | 2.6 | 1 |
| PA61M | * | 38 | 7 | * | * | 6 | 65 | 30 | * | * | * | * |
| PA61 | * | * | * | * | * | * | * | * | * | * | * | * |
| PA51A[3] | 10 | 32 | 8 | 10/40 | 97 | 5 | 40 | 20 | 10 | 16 | 2.6 | 1 |
| PA51M | * | * | * | * | * | 10 | 65 | 40 | * | * | * | * |
| PA51 | * | 28 | * | 10/36 | * | * | * | * | * | * | * | * |
| PA07A | 5 | 45 | 5 | 12/50 | 67 | .5 | 10 | .01 | 30 | 18 | 5 | 1.3 |
| PA07 | * | * | * | * | * | 2 | 30 | .05 | * | * | * | * |
| PA07M | * | * | * | * | * | * | * | * | * | * | * | * |
| PA10A | 5 | 44 | 6 | 10/50 | 67 | 3 | 40 | 20 | 30 | 23 | 5 | 6 |
| PA10M | * | 37 | 8 | 10/45 | * | 6 | 65 | 30 | * | * | * | * |
| PA10 | * | * | * | * | * | * | * | * | * | * | * | * |
| PA11 | 5 | 22 | 8 | 10/30 | 67 | 10 | 65 | 40 | 30 | 23 | 2.6 | 1 |
| PA73[3] | 5 | 22 | 8 | 10/30 | 67 | 10 | 65 | 40 | 5 | 23 | 2.6 | 1 |
| PA73M | * | * | * | * | * | * | * | * | * | * | * | * |
| PA01 | 5 | 18 | 10 | 10/28 | 67 | 12 | 65 | 50 | 50 | 23 | 2.6 | 1 |
| PA02A | 5 | 15 | 4 | 7/19 | 48 | 3 | 25 | .1 | 37 | 350 | 20 | 4.5 |
| PA02M | * | * | * | * | * | 10 | 50 | .2 | 40 | * | * | * |
| PA02 | * | * | * | * | * | * | * | * | 37 | * | * | * |
| PA09A | 2 | 32 | 8 | 10/40 | 78 | .5 | 10 | .02 | 85 | 2500 | 400 | 75 |
| PA09M | * | * | * | * | * | 3 | 30 | .1 | * | * | * | * |
| PA09 | * | * | * | * | * | * | * | * | * | * | * | * |
| PA12H | 1 | 41 | 4 | 45 | | 6 | | 30 | 100 | | | |
| PA08A | .15 | 135 | 10 | 15/150 | 17.5 | .5 | 10 | .01 | 8.5 | 90 | 30 | 5 |
| PA08M | * | * | * | * | * | 2 | 30 | .05 | * | * | * | * |
| PA08 | * | * | * | * | * | * | * | * | * | * | * | * |
| PA83A | .075 | 140 | 10 | 15/150 | 17.5 | 1 | 10 | .01 | 8.5 | 60 | 30 | 5 |
| PA83M | * | * | * | * | * | 3 | 25 | .05 | * | * | * | * |
| PA83 | * | * | * | * | * | * | * | * | * | * | * | * |
| PA80J | .06 | 30 | 5 | 15/35 | 11.5 | 10 | 30 | .05 | 10 | 100 | 15 | 5 |
| PA84A | .04 | 143 | 7 | 15/150 | 17.5 | 1 | 10 | .01 | 7.5 | 250 | 200 | 75 |
| PA84M | * | * | * | * | * | 3 | 25 | .05 | * | * | * | * |
| PA84 | * | * | * | * | * | * | * | * | * | * | * | * |
| PA84S | * | * | * | * | * | * | * | * | * | * | * | * |
| PA81J | .03 | 70 | 5 | 32/75 | 11.5 | 3 | 25 | .05 | 8.5 | 60 | 20 | 5 |
| PA82J | .015 | 145 | 5 | 70/150 | 11.5 | 3 | 25 | .05 | 8.5 | 30 | 20 | 5 |

# ORDER OF PERFORMANCE FOR OTHER PARAMETERS

| Slew Rate V/µs Typ** | | PWR BW @ NOM $V_{out}$ KHz[2] Typ** | | $V_S$-Out Delta V Max | | Voltage Offset mV Max | | $V_{offset}$ vs Temp µV/°C Max | | Settling Time .1% µs Typ | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PA09 | 400 | PA09 | 2500 | PA02** | 4 | PA07A, 08A, 09A | .5 | PA07A, 08A, 09A | 10 | PA09** | |
| PA84 | 200 | PA02 | 350 | PA07**, 80J | 5 | PA83A, 84A, 03A | 1 | PA83A, 84A, 03A | 10 | PA02** | |
| PA08, 83 | 30 | PA84 | 250 | PA81J, 82J | 5 | PA07(M), 08(M) | 2 | PA02A, 83, 84, 81J, 82J | 25 | PA84S | |
| PA02, 81J, 82J | 20 | PA80J | 100 | PA12, 12M | 6 | PA02A, 03, 09(M), 81J | 3 | PA03, 07, 08, 09, 80J | 30 | PA08** | |
| PA80J | 15 | PA08 | 90 | PA10A | 6 | PA10A, 12A, 83(M), 82J | 3 | PA10A, 12A, 51A, 61A | 40 | PA07** | 1 |
| PA03 | 8 | PA83, 81J | 60 | PA03** | 7 | PA84(M,S), 61A | 3 | PA02 | 50 | PA01, 03** | |
| PA07, 10 | 5 | PA03 | 50 | PA84**, 12A | 7 | PA51A | 5 | PA01, 10(M), 11, 12(M) | 65 | PA10**, 11 | |
| PA12 | 4 | PA82J | 30 | PA10, 10M | 8 | PA10(M), 12(M), 61(M) | 6 | PA51(M), 61(M), 73(M) | 65 | PA12** | |
| PA01, 11 | 2.6 | PA01, 10 | 23 | PA09**, 11 | 8 | PA02, 11, 51(M) | 10 | | | PA51, 61** | |
| PA51, 61 | 2.6 | PA11, 73 | 23 | PA51, 73** | 8 | PA73, 80J | 10 | | | PA73** | |
| PA73 | 2.6 | PA12 | 20 | PA01, 08** | 10 | PA01 | 12 | | | PA83** | |
| | | PA07 | 18 | PA83** | 10 | | | | | PA84(A,M) | 1 |
| | | PA51, 61 | 16 | | | | | | | PA80J, 81J, 82J | 1 |

| $V_{os}$ Adj | Current Limit | Thermal Shutdown | Input Stage | Temp Range Max | Second Source[1] |
|---|---|---|---|---|---|
| Yes | Thermal | Yes | FET | 25/85 | No |
| * | * | * | * | * | * |
| No | Ext Adj | No | Bipolar | −55/125 | Direct |
| * | * | * | * | * | No |
| * | * | * | * | −25/85 | Direct |
| No | Ext Adj | No | Bipolar | −25/85 | No |
| * | * | * | * | −55/125 | * |
| * | * | * | * | −25/85 | * |
| No | Ext Adj | No | Bipolar | −55/125 | Direct |
| * | * | * | * | * | * |
| * | * | * | * | −25/85 | * |
| Yes | Ext Adj | Yes | FET | −25/85 | Possible |
| * | * | * | * | * | * |
| * | * | * | * | −55/125 | * |
| No | Ext Adj | No | Bipolar | −55/125 | Possible |
| * | * | * | * | * | * |
| * | * | * | * | −25/85 | * |
| No | Ext Adj | No | Bipolar | −25/85 | Direct |
| No | Ext Adj | No | Bipolar | −25/85 | Direct |
| * | * | * | * | −55/125 | No |
| No | Ext Adj | No | Bipolar | −25/85 | Possible |
| No | Ext Adj | No | FET | −55/125 | Similar |
| * | * | * | * | * | * |
| * | * | * | * | −25/85 | * |
| Yes | 4.5 | Yes | FET | −25/85 | No |
| * | * | * | * | −55/125 | * |
| * | * | * | * | −25/85 | * |
| No | Ext Adj | No | Bipolar | −25/200 | No |
| Yes | Ext Adj | Yes | FET | −25/85 | No |
| * | * | * | * | 55/125 | * |
| * | * | * | * | −25/85 | * |
| Yes | 1A | Yes | FET | −25/85 | Possible |
| * | * | * | * | −55/125 | No |
| * | * | * | * | −25/85 | Possible |
| Yes | .1A | Yes | FET | 0/70 | Direct |
| Yes | .05A | Yes | FET | −25/85 | Possible |
| * | * | * | * | −55/125 | No |
| * | * | * | * | −25/85 | Possible |
| * | * | * | * | * | No |
| Yes | .05A | Yes | FET | 0/70 | Direct |
| Yes | .025A | Yes | FET | 0/70 | Direct |

**NOTES:**

*Specification is the same as above.
**Applies to all grades of the model.

1. Second source explanation:
   Direct = All major specification are equal.
   Possible = Pin for pin but differences in specifications.
   The APEX part is usually superior in one or more parameters.
   Similar = External connections and specifications are similar.
2. Higher frequencies are possible at reduced output levels.
3. Class "C" outputs are optimized for low cost - not recommended above 1KHz.



# CUSTOMIZING POWER OP AMPS

APEX does customize standard models to meet specific customer requirements. Available options range from custom marking through minor internal circuit changes. Custom orders usually involve a minimum quantity, a per shipment lot charge, and a per piece surcharge over the cost of the standard model. The following are examples of services performed.

- Standard part plus burn in
- Disconnect thermal shutoff
- Test drift over wider temperature range
- Grade out for improved voltage drift
- Customer part numbers up to 10 digits
- Gold flashed pins in place of nickel
- Provide individual test data
- Non-standard quiescent current trim

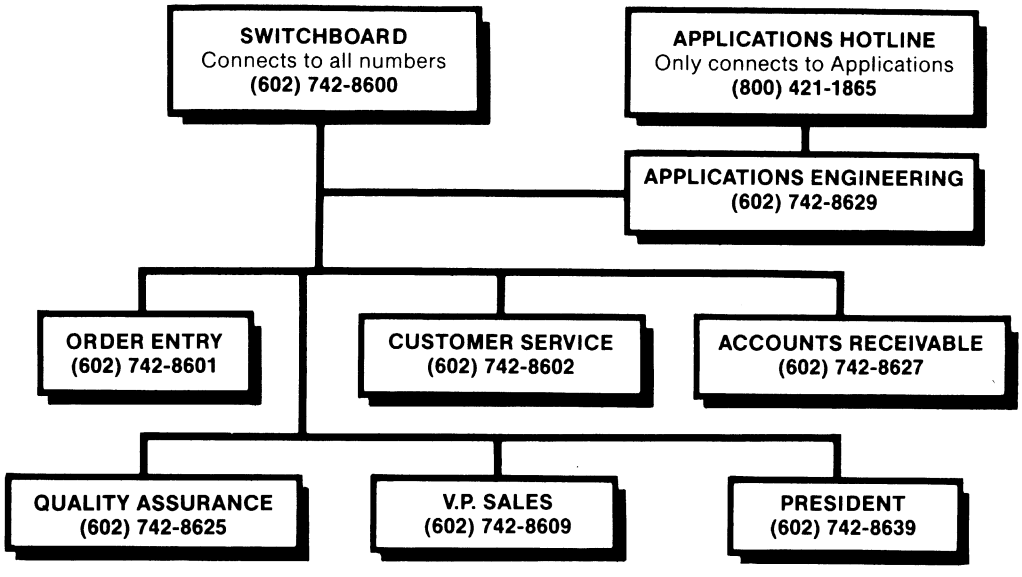
The "Q" option has proven to be very cost effective when reliability is of great concern but economic factors do not allow the use of military screened parts. "Q" parts carry specifications identical to the corresponding non-"A" model but are screened as follows prior to complete electrical testing:

- Stabilization bake, 24 hours at 150°C
- Temperature cycle, (10), −65 to 150°C
- Constant acceleration, 10,000G, Y1 axis
- Fine leak test, 1E-7 cc/S max.
- Gross leak, test 60 PSI pressurization
- Burn-in, 160 hours at 125°C

To discuss a custom option for your application, call the APEX Applications Hotline (800) 421-1865 or (602) 742-8629.

# ACCESS DIRECTORY

## TELEX: 170631



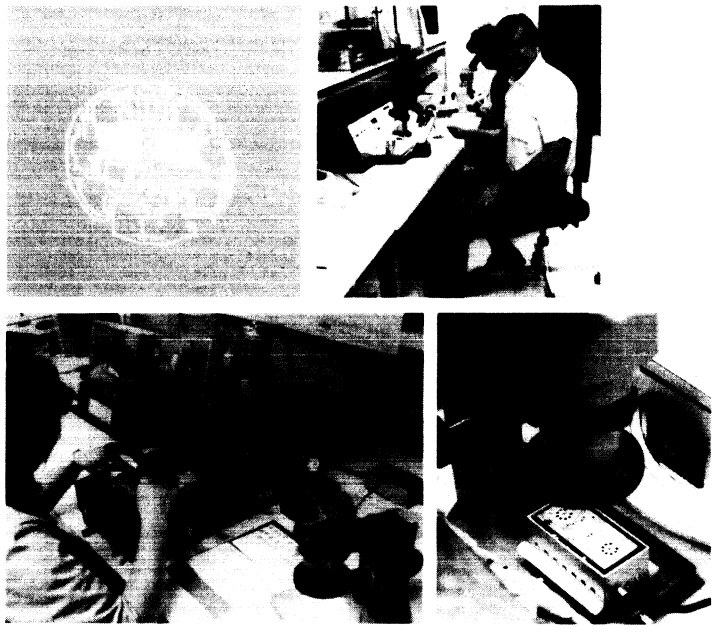

## STANDARD HOURS:

| | MOUNTAIN STANDARD TIME | GREENWICH MEAN TIME |
|---|---|---|
| SWITCH BOARD: | 8:00 AM to 4:30 PM | 15:00 to 23:30 |
| ORDER ENTRY: | 7:00 AM to 5:00 PM | 14:00 to 24:00 |
| OTHER: | 8:00 AM to 4:00 PM | 15:00 to 23:00 |

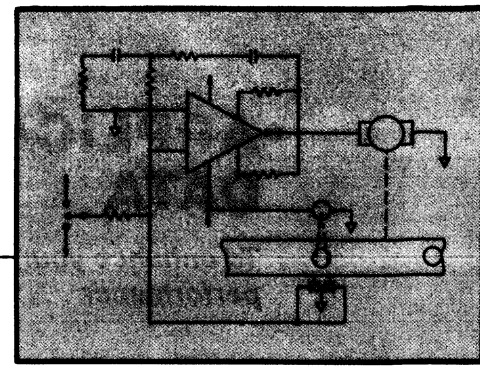
**APEX MICROTECHNOLOGY CORP. (Domestic)**
**APEX F.S.C. INC. (Export)**
5980 N. SHANNON ROAD, TUCSON, AZ 85741, USA

# •APPLICATIONS DATA

***To enhance your circuit performance . . .***



*(800) 421-1865*



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*The APEX Applications Hotline is the quickest way to get answers about your specific circuit needs. It puts you in touch with a wealth of experience from the world over.*

*Technical seminars are given across the U.S. and around the free world. They provide extensive information on power op amp applications in addition to the hows and whys of internal circuits and construction. Pros and cons of various approaches are presented along with potential dangers. Question and answer periods can emphasize areas of special interest. These seminars are available to groups of 10 or more engineers interested in power op amps. Contact your local representative or myself about the schedule in your area.*

*Application notes are developed with the help of your questions, suggestions and feedback. Please call me if you have identified and implemented a new, useful application and are ready to share the information with others. You may be eligible for a $250 reward.*

Granger Scofield

**GRANGER SCOFIELD**
**V.P., MARKETING**
**(602) 742-8629**

# THE ADVANTAGES OF IC POWER OP AMPS

*by Granger Scofield*

The power op amp, also referred to as the power operational amplifier, is one of the most fascinating inventions of the electronics industry. Advanced manufacturing techniques enable a wide variety of industries to reduce cost and/or enhance quality and performance of goods and services. This rapidly growing technology has provided a great business opportunity to manufacturers willing to provide technical information and give applications support to those who are designing tomorrow's machines.

## EVOLUTION OF THE POWER OP AMP

In the May 1947 proceedings of IRE, "Analysis of Problems in Dynamics by Electronic Circuits" discussed a new form of electronic circuit used to aid the analysis of real world mechanical problems. It was named the operational amplifier (op amp) for its ability to perform math operations such as adding, subtracting, multiplying, integrating and differentiating. As the name implies, op amps are specialized types of amplifiers which fit the more general definition of an amplifier: Current or voltage control devices used to increase the strength of an electrical signal.

The op amp forms a very flexible general purpose gain block. By adding two or three passive components it can achieve many desired functions which are then controlled by the external components rather than the op amp. This makes the op amp very easy to use compared to the design effort required to implement circuits starting with a hand full of transistors.

The op amp consists of a differential input stage, intermediate stages as required, and the output stage. The differential input stage is a major distinguishing feature of the op amp. The internal circuitry is arranged to insure that errors of individual transistors cancel each other. External components are arranged so that the op amp is always amplifying the difference between the input and output signals, thereby comparing the real output to the desired output. This produces accuracy levels which are not attainable using other types of amplifiers.

The high accuracy levels and great flexibility of the op amp have led to volume production and large expenditures in the area of research and development to both improve performance and lower cost. The original designs which utilized several vacuum tubes for each amplifier have given way to integrated circuit technology in the same manner that today's pocket calculators have more computing power than the early computers which filled whole buildings.

Within the field of op amps, specializations are growing daily. High speed op amps are being used to process television signals, high voltage op amps drive ink jet printers, high current op amps control guided missile fins, and high accuracy op amps control industrial processes with high precision. Op amps operating on total supply voltages above 44V and which can deliver currents above .1A comprise what is known as power op amps. We will examine some specifics which must be considered when deciding whether to purchase a power op amp or design a circuit starting with individual transistors.

While power op amps obey all the rules associated with the general op amp family, their construction is often quite different from their low power counterparts. The vast majority of today's op amps are single integrated circuits with a suitable package. Simpler power op amps consist of one of these integrated circuits as a front end plus the high current output stage housed in a package suitable for high power dissipation. Units of this simple construction are usually limited to the operating voltage of today's ICs (up to 100V).

A more complex construction method is predominant in high voltage units (over 100V). Many individual transistors in chip form are assembled to make up the amplifier. Due to the larger number of components and increased labor costs of assembly, such a device usually costs more than units using the simpler technique. However, in addition to the high voltage rating achieved, accuracy specifications of these amplifiers tend to be better due to improved control of individual devices and laser trimming of the input stage.

## APPLYING POWER OP AMPS

Fig. 1 illustrates the use of a power op amp. It shows two diagrams satisfying the drive requirements of a computerized speaker test set. Both circuits will deliver 25W of audio power with very low distortion levels. However, the circuits vary substantially in cost related primarily to the parts count of 11 for the power op amp circuit and 27 for the discrete version. Our analysis will take into consideration design costs, incremental costs, production run costs and performance.

First let us consider the cost of the actual circuit design. Each component's value, tolerance and suitability must be established. Whether this calculation is quick or lengthy depends on the designer's experience. Extensive computer analysis may be required. If a power op amp is used, the lower parts count and the rather well known design rules help reduce circuit design time by more than half. If written repair procedures are required, a similar reduction in time would occur. After specific components are chosen, preparation of component specifications, incoming inspection procedures, procurement procedures, and inventory management must follow. These peripheral tasks all decrease with lower component counts of a design based on a power op amp.

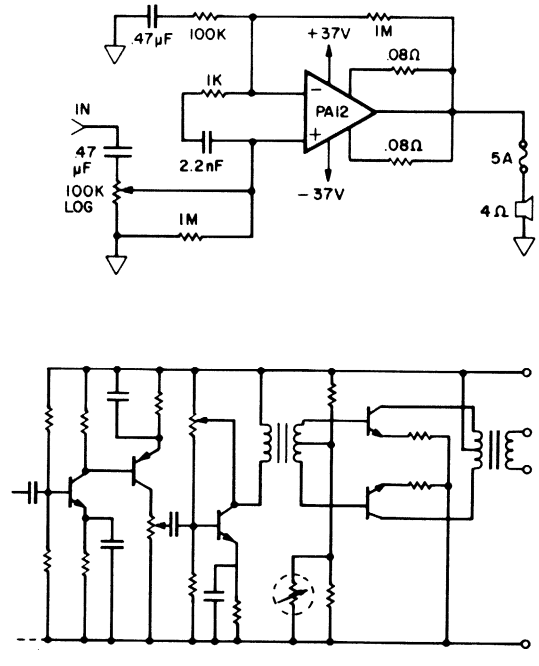



FIG. 1

The second cost factors are those relating to the incremental production costs. Total components costs for the op amp design may exceed those of the discrete design, but this is only one part of the finished goods cost. By far, the most expensive assembly operations are the mounting of the power devices and the hardware to keep them cool. The power op amp design costs amount to half of the discrete counterpart due to half the power package count. In addition, some power op amps provide internal thermal sense circuitry.

Logistics costs must be considered as groups of parts are ordered for a production run. Purchase orders often cost $25 or more to process. Incoming inspection needs to test parts as they are received. As you go on to consider inventory costs and accounting costs in both purchasing and accounting, the lower number of components required by the power op amp design significantly reduces overall costs.

Although much harder to estimate, features of reliability, size and weight definitely affect the performance and quality of any product. It may be possible to build a hybrid power op amp with exactly the same transistors used in a discrete design, but all three of the above features can be improved. The concept of size and weight reduction are quite obvious and can be visualized when viewing the diagrams of the two design approaches. These diagrams also show the hybrid power op amp having considerably fewer interconnections, thus increasing reliability.

## MAJOR ADVANTAGES OF IC CONSTRUCTION

The improved reliability of the op amp design is illustrated in Fig. 2 which shows the biasing network for the output stage of the op amp. R1, R2 and Q2 form a $V_{BE}$ multiplier to establish the class A-B biasing for Q1 and Q3. A minimum level of bias (class A-B) is required to maintain adequate distortion levels for the speaker test set. Transistor therory holds that the base-emitter voltage ($V_{BE}$) decreases as temperature rises. If the bias voltage were fixed, quiescent current would increase radically with temperature causing over heating of Q1 and Q3. This in turn would lead to more current and thermal runaway. Thermal runaway can be avoided by increasing the value of R3 and R4 substantially. However, these resistors are in series with the load where they waste power. Extra power must be supplied by the main power supply through Q1 and Q3, in effect, raising system power levels and heat generation.

The most elegant way to cure the runaway problem is to thermally couple Q2 and Q1 and Q3. As a result, the increased temperature of the transistors will cause a decrease in the bias level because the $V_{BE}$ of Q2 matches the $V_{BE}$ of the power transistors. Such tight thermal coupling can be implemented by having the $V_{BE}$ junction of Q2 close to the actual heat producing junction of the power transistors. This is physically possible only with microcircuits. In addition, high performance hybrid power op amps also include a network of temperature variable resistors in the $V_{BE}$ multiplier circuit. This insures even better tracking of the power transistor $V_{BE}$ levels.

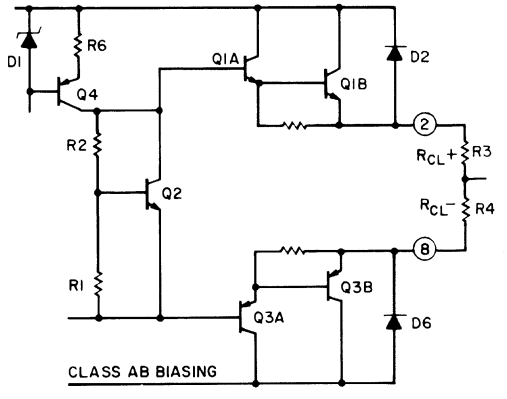



**FIG. 2**

The same physical closeness also allows reliable thermal protection. The closer the sensor is to the heat source, the easier it is to control the temperature of that source. Power op amps with thermal shutdown, have the sensing element placed very close to the power transistors. In APEX MICROTECHNOLOGY's newest amplifiers, this element is placed directly on top of the power transistor. This results in a two millisecond response time with near zero temperature difference between the heat source and the sensing element.

## CONCLUSION

In examining the construction of a hybrid power op amp, it is apparent that vast advantages come to light when this device is considered as an alternative to a discrete design. One advantage is having most components inside a single package. More significant are the assets inherent in the hybrid construction. Most important, is very tight thermal coupling between the power output stage and the biasing stage. For these reasons the power op amp has become a successful product and a key choice used by many in the electronics industry.

# POWER OPERATIONAL AMPLIFIER APPLICATIONS NOTE 1
## GENERAL OPERATING CONSIDERATIONS

### INTERPRETING SPECIFICATIONS

Absolute maximum ratings are stress levels which when applied to the amplifier one at a time will not cause permanent damage. However, proper operation is only guaranteed over the ranges listed in the specifications table. For example, most amplifiers have an absolute maximum case temperature range of −55 to 125°C. If the operating temperature range is less (ie. −25° to 85°) an amplifier may latch to one of its supply rails when above that temperature (>85°C); however, the device will not sustain permanent damage unless the latched condition also violates the safe operating area. Simultaneous application of two or more of these maximum stress levels such as maximum power and temperature may induce permanent damage to the amplifier.

The absolute maximum power dissipation rating used by APEX is the generally accepted industry method which assumes the case temperature of the amplifier is held at 25°C and the junctions are operating at the absolute maximum rating. This standardization provides a yardstick when comparing ratings of various manufacturers. However, this is not a reasonable operating point because it requires an ideal heatsink. Furthermore even with the best heatsink, it would still result in reduced product life due to operation at extreme temperatures. Refer to the heatsink data sheet for information regarding operating junction temperatures and relative product life. APEX generally recommends maximum junction temperatures at 150° or below.

The specifications table should be the prime working document while designing the application. In addition to the minimum/maximum parameters (voltage offset, output capability, etc.) this table contains the guaranteed linear operating ranges (common mode voltage, temperature, power supplies, etc.).

Common mode voltage is another case which points out the difference between absolute maximums and linear operating range. On many amplifiers, the maximums allow inputs up to the power supply rails, while the linear operating range is 5-10V less than the power supply rails. This means inputs exceeding the linear range specification will not damage the part but the amplifier may not achieve the specified rejection ratio, start to distort the signal or may even latch to one of the supply rails.

### STABILITY

Oscillations not only destroy signal fidelity but can cause catastrophic failures due to increased power dissipation. Oscillations caused by ground loops, inadequate supply bypassing or high impedance input nodes often are in the megahertz range and can easily be overlooked because the circuit is designed for low frequency operation. When testing the circuit, oscilloscope settings need to be adjusted to detect the presence of any high frequency oscillations. If present, reactive elements of the load can increase current drawn from the amplifier (capacitive load). What is worse, the current is not the phase with the output voltage further increasing the internal power dissipation.

To prevent oscillations, a reasonable phase margin must be maintained. The low pass created by sumpoint (−IN) capacitance and the feedback network may add phase shift and cause instabilities. As a general rule, the sumpoint load resistance (input and feedback resistors in parallel) should be selected so that the low pass breakpoint with the input and stray capacitance in parallel is at least 10 times the small signal bandwidth of the circuit. The external sumpoint stray capacitance to common, $+V_S$ or $-V_S$ should be kept at an absolute minimum.

Low impedance at the noninverting input (+IN) is equally important to prevent pickup of unwanted signals or even positive feedback. Capacitance to common (or a supply rail) is often helpful to eliminate the problem.

### IMPROVING STABILITY

In applications where long cables or highly reactive loads are used but the bandwidth is not critical, instabilities can be eliminated by reducing the feedback at the high frequency end. This is done by adding a series RC network across the inputs as shown in Fig. 1. The value of the resistor ($R_N$) should be selected for a ratio of one tenth (1/10) to one hundredth (1/100) of $R_F$ and the capacitance should be chosen for a corner frequency of less than one tenth (1/10) to one hundredth (1/100) of the small signal bandwidth of the amplifier respectively. Typical values are:

| SMALL SIGNAL BW | RATIO | $F_C$ | $R_F$ | $R_N$ | $C_N$ |
|---|---|---|---|---|---|
| 5 MHz | 1/100 | 50KHz | 10K | 100 | 33nf |
| 1 MHz | 1/10 | 100KHz | 10K | 1K | 1.5nf |

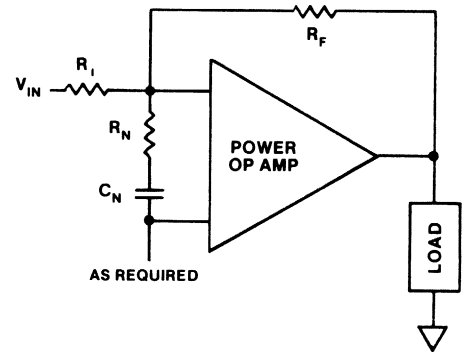



**FIGURE 1. INCREASED STABILITY**

This RC network can sometimes be used to increase the slew rate of externally compensated high speed Power Op Amps when requiring high speed at a low gain setting because the product data sheet will prescribe an external phase compensation which will reduce slew rate. By applying the RC network above, the AC gain of the amplifier is increased thereby allowing the compensation for a higher gain setting, thus increasing slew rate and bandwidth. Application note 3, Figure 3 illustrates this technique using the PA84 as an electro-static deflection amplifier.

### SUPPLY VOLTAGE

The specified voltage ($+/-V_S$) applies for a dual (+/−) supply having equal voltages. A nonsymmetrical (i.e. +50/−10V) or a single supply (i.e. 60V) may be used as long as the total voltage between $+V_S$ and $-V_S$ does not exceed the maximum rating.

### SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The secondary breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceed specific limits. (Does not apply for MOS output transistors.)
3. The junction temperature of the output transistors.

The SOA curves for the model to be used combine the effect of these limits. The direction and magnitude of the output current must be calculated or measured and checked against these curves. The direction of current flow determines which op amp output transistor is conducting and thus which supply voltage to use when calculating the supply to output differential.

The direction of the output current is obvious for purely resistive loads but not for reactive or EMF producing loads which often cause problems. For example, consider a power op amp running on ±28V with a large capacitive load. Assume the output voltage is near the negative supply rail and switches to the positive rail. The output transistor connected to the positive supply rail turns on the supplies current to the capacitor. Initially, the capacitor is charged to the negative output voltage and appears as a near short circuit. This places a voltage stress of twice the supply voltage on the power transistor (nearly 56V in this case).

## CURRENT LIMIT ADJUST

Power Op Amps with provisions to adjust current limit externally require two current limit resistors ($R_{CL}$) which must be connected as shown in the applicable external connection diagram. Since output current flows through these resistors, wattage ratings must be considered. For optimum reliability, the resistor values should be set as high as possible. Each resistor and its power dissipation is calculated as follows:

$$R_{CL}\ (\Omega) = 0.65/I_{LIM}(A) - 0.01^{*} \qquad P(W) = 0.65 \times I_{LIM}$$

*Except for PA12, replace by 0.007

Nonsymmetrical current limiting ($R_{CL+} \neq R_{CL-}$) is permissible. For testing without heatsink, the resistors should be selected to limit power dissipation to less than 3W under short circuit conditions.

The external current limiting for the power op amps is not meant to be a precision current limit. A rule of thumb is to allow ±20% variation at room temperature. Furthermore, the current limit varies over temperature. This variation is generally shown in a typical performance graph in the product data sheet. Specific values of the nominal current at any given temperature may be calculated by modifying the 0.65V term of the above equation with −0.0022V/°C of case temperature rise. For example, at a case temperature of 125°C, this term becomes 0.43V rather than 0.65V. When working with high currents, connection impedances, lead lengths and solder joint resistances must be included when calculating the current limit.

## HEATSINK

The amplifier may be operated without a heatsink only if the internal power dissipation is less than 3W at 25°C ambient. To determine the heatsink requirements for any application, follow this procedure:

1. Calculate the maximum DC or instantaneous power dissipation:

$$P = (V_S - V_O)\, I_O + (\,|\,+V_S\,|\,+\,|\,-V_S\,|\,)\, I_Q$$

2. Determine the maximum junction temperature ($T_J$) and thermal resistance of the Power Op Amp to be used and thermal resistance of the interface between heatsink and case of the amplfiier (0.2°C/W for TO-3 packages mounted with thermal grease and without insulating washers). The technical notes section of the Heatsink data sheet discusses relative product life as a function of operating temperature, thermal properties of the mounting interface and mounting recommendations.

3. Calculate the minimum thermal resistance of the heatsink:

$$\Phi_{HS} = \frac{T_J - T_A\ (°C)}{P\ (W)} - \Phi_{JC} - \Phi_{HSC}$$

## GROUNDING

Since the case is electrically isolated (floating) with respect to the internal circuits it is recommended to connect it, or the heatsink it is mounted on, to a local signal common. As an alternative, this connection may be AC coupled; i.e. mounting the amplifier side-by-side with a non-insulated hot case regulator (providing the regulator case terminal is well bypassed to common). Single point grounding of the input resistors and signal to common will prevent undesired current feedback, which can cause large errors and/or instabilities.

## SINGLE SUPPLY OPERATION

These amplifiers are suitable for operation from a single supply voltage. The operating requirements do however, impose the limitation that the input voltages do not approach closer than 5 to 10V volts to either supply rail. Specific values are determined by the common mode voltage range given in the product data sheet. This is due to the internal operating voltage requirements of the power op amp current sources, the half-dynamic loads and the cascode stage. Thus, single supply operation requires the input signals to be biased at 5 to 10V from either supply rail. Figure 2 illustrates one bias technique to achieve this.

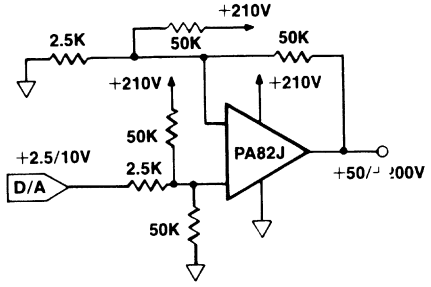



**FIGURE 2. TRUE SINGLE SUPPLY OPERATION.**

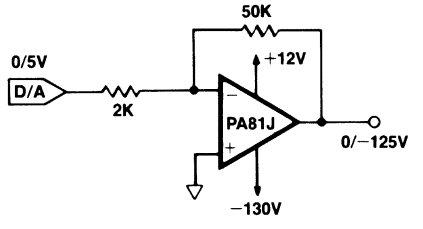



**FIGURE 3. NON-SYMMETRIC SUPPLIES.**

Figure 3 illustrates a very practical deviation from true single supply operation. The availability of the second low voltage supply still allows ground (common) referenced signals but also maximizes the high voltage capability of the unipolar output. This technique can utilize an existing low voltage system power supply and does not place large current demands on that supply. The 12 volt supply in this case must supply only the quiescent current of the Power Op Amp. If the load is reactive or EMF producing, the low voltage supply must also be able to absorb the reverse currents generated by the load.

## BYPASSING OF SUPPLIES

Unless the leads to the power supply are less than 2" long, each supply rail should be bypassed to common with a capacitance of 10μF per Ampere of peak output current physically connected less than 2" from the power supply pins. Capacitors over 0.22μF should be made up of a 0.22μF ceramic capacitor in parallel with additional tantalum capacitors. For operating temperatures above zero °C computer grade aluminum electrolytic capacitors may be adequate.

## SYMBOLS USED

| | |
|---|---|
| $C_N$ | :External Rolloff Capacitor |
| $I_{LIM}$ | :Current Limit |
| $I_O$ | :Output Current |
| $I_Q$ | :Quiescent Current |
| P | :Power |
| $R_{CL}$ | :Current Limiting Resistor |
| $R_F$ | :Feedback Resistor |
| $R_I$ | :Input Resistor |
| $R_L$ | :Load Resistor |
| $R_N$ | :External Rolloff Resistor |
| $\Phi_{HS}$ | :Thermal Resistance of Heatsink |
| $\Phi_{HSC}$ | :Thermal Resistance from Heatsink to Case |
| $T_C$ | :Case Temperature |
| $T_A$ | :Air Temperature (ambient) |
| $T_J$ | :Junction Temperature (Desired Max) |
| $V_{IN}$ | :Input Voltage |
| $V_O$ | :Output Voltage |
| $V_S - V_O$ | :Supply to Output Differential Voltage (Internal V-Drop) |
| $V_S$ | :Supply Voltage |

# POWER OPERATIONAL AMPLIFIER APPLICATIONS NOTE 2

## OPTOELECTRONIC POSITION CONTROL

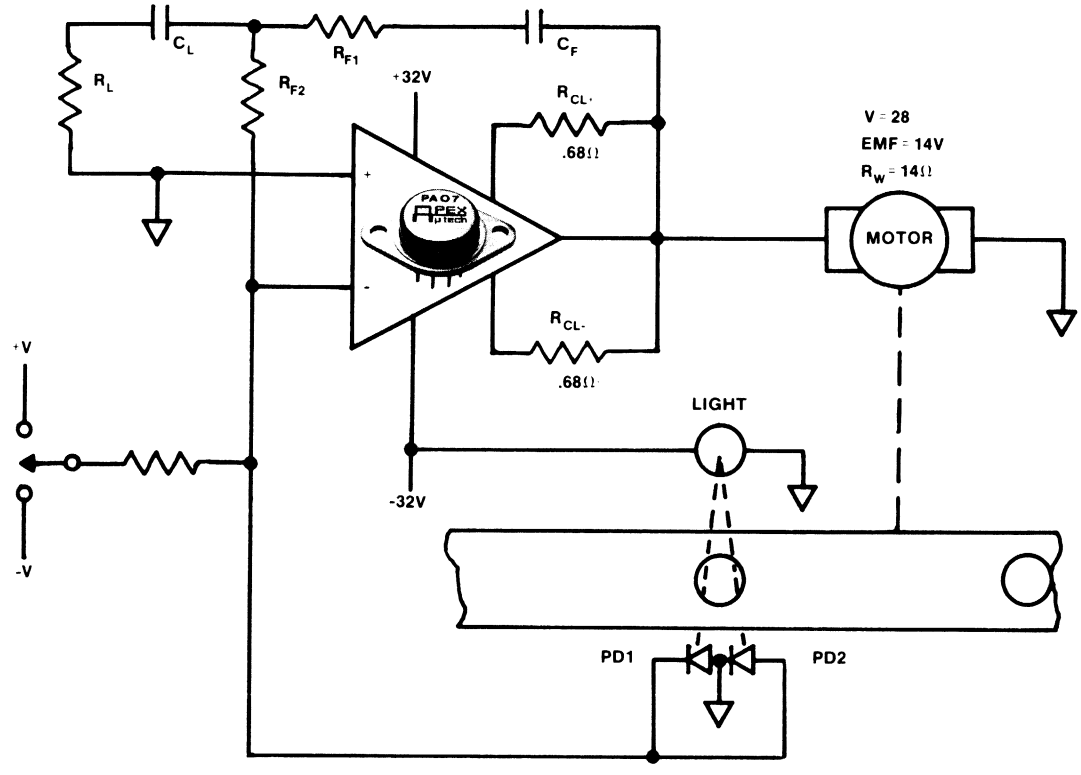



FIG. 1 SEQUENTIAL POSITION CONTROL

## INTRODUCTION

Power Op Amps are ideally suited for position control because their response time is fast compared to any mechanical drive train. The optoelectronic technique of position control can move to and maintain fixed index points on linear or rotary motion components while adding no linkages or independently moving parts. The resulting system features high reliability, accuracy and repeatability. If the integration of photodiode currents is required, select a power amplifier with an FET input to maintain very low bias current levels such that the integrating capacitor voltage will remain constant during periods when both photodiodes are not illuminated. Further selection criteria should be based on motor ratings and/or available power.

## SEQUENTIAL POSITION CONTROL

In the circuit shown in figure 1, the PA07 integrates the differential output of the pair of photodiodes and drives the motor in the proper direction until the photodiode currents are equal. This differential configuration negates the well known temperature and time instabilities of optoelectronic devices. To move between index points, a fixed input current is momentarily switched to the amplifier input causing the amplifier to drive the motor in the desired direction. The charge on $C_F$ will maintain motor drive as the input current is switched off prior to reaching the index point. As the first photodiode is illuminated, its output reinforces the current direction of motion. As the second photodiode is illuminated, its current will reverse the motor drive, causing the system to lock to the index point.

As motor response and system inertia vary widely, $C_F$ and $R_F$ must be selected for the individual application to provide proper damping. $C_F$ must be small enough to allow drive reversal before the index point passes the second photodiode or the system will continue on to the next index. Very small values of $C_F$ can cause severe overshoot or oscillation leading to motor burnout and/or drive train failure. $R_{F_1}$ and $R_{F_2}$ are required to stabilize the control loop at the unity gain point and to minimize overshoot. $R_L$ and $C_L$ form a lead network which may be included to improve response time by enabling the amplifier to modify the motor drive based on a change of the sensor output. In this manner a braking force can be applied to the motor prior to reaching the index point. The motor shown, having EMF of 14V will apply a 46V stress across the conducting output transistor when reversed. With a duration longer than 5ms, the steady state secondary breakdown line of the SOA for the PA07 (see data sheet) curves requires the current limits to be set to 1A.

## SINGLE POINT POSITION CONTROL

A variation of the above technique shown in figure 2 can be used to return a wheel to a single index point after rotating in either direction. The low inertia, fast response system will take the shorter route to the index point when switched from run to stop. The PA12A was selected for this application because it provided high power while keeping bias current levels low with respect to the photodiode currents. To improve response time, the lead network compensates for motor response lagging behind any change in drive voltage. A run control current of sufficient amplitude to override the photodiode currents is fed to the amplifier inverting input. Removal of this current restores control to the photosensors.

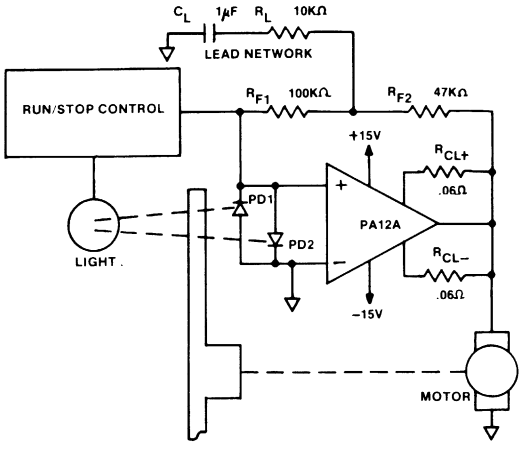



FIG. 2 SINGLE POINT POSITION CONTROL

## POSITION CONTROL MASK

Figure 3 shows details of the wheel preparation and sensor placements at the stop index. Arrows indicate direction of rotation when the corresponding photodiode has the higher output. While it is theoretically possible to achieve a stable position on the opposite side of the wheel, system noise or a slight movement will imbalance the equal photodiode currents and the higher current sensor will receive even more light causing the wheel to seek the desired index point. Masking of the wheel at an angle to the radial softens the control function and prevents overshoot.

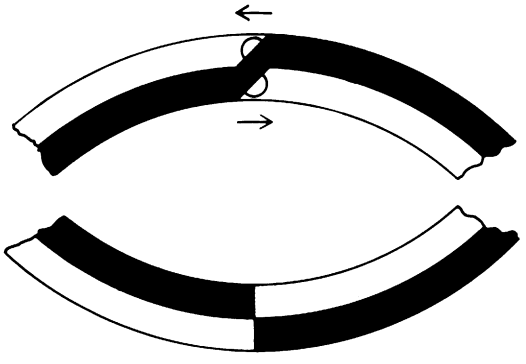


FIG. 3 SINGLE INDEX POINT DISK

## SPOT SIZE

Optimum relationship of beam size to active areas of the photodetectors is shown in figure 4. A centered beam should illuminate half the photosensitive area of each diode. Too large a beam will produce no change of sensor output for a range of positions, while a smaller beam will produce a nonlinear transfer function near the center line between the photosensitive areas. This makes selection of $C_F$ to dampen the circuit become difficult and requires a higher intensity light source.

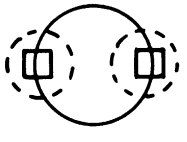


FIG. 4 BEAM-SENSOR ALIGNMENT

## DIGITAL INTERFACING

For systems with digital control figure 5 illustrates a method not requiring generation of bipolar control signals thus saving the cost of digital to analog conversion. When logic lines are low the signal diodes will not conduct leaving control to the photodiodes. A high level on line 2 will cause current to flow to the summing junction and the amplifier will swing negative. A high level on line 1 will raise the summing junction voltage above ground, and the amplifier will swing positive. Select a resistance value such that a high logic level will provide at least twice the maximum current from each photodiode to insure control override regardless of photodiode signals.

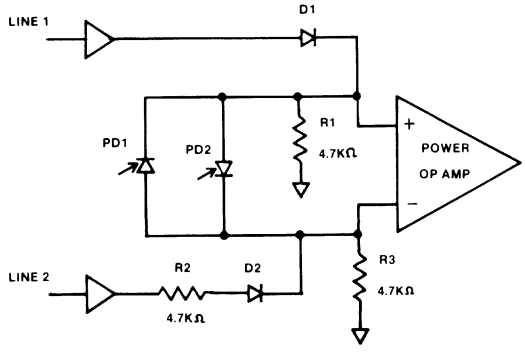



FIG. 5 DIGITAL INTERFACE

## DUAL SENSORS

For applications requiring high precision, the use of a dual element position sensing photodetector[1] will allow smaller beam size, tighter beam control and provide better thermal equilibrium. The specified resolution of the detector recommended for this application is better than .0127mm (.0005 inch). The detector is a three terminal device requiring a current inverter as shown in figure 6 to achieve the differential configuration. Two equal resistors, R1 and R2, should be scaled to the maximum photodiode current and swing capability of the signal amplifier.

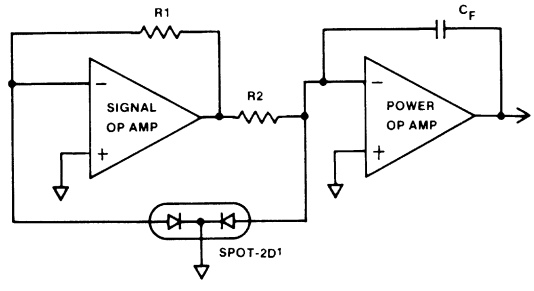



FIG. 6 CURRENT INVERSION

NOTE[1]: A line of multi-element position sensors is available from:
United Detector Technology
3939 Landmark Street
Culver City, CA 90230
(213) 204-2250

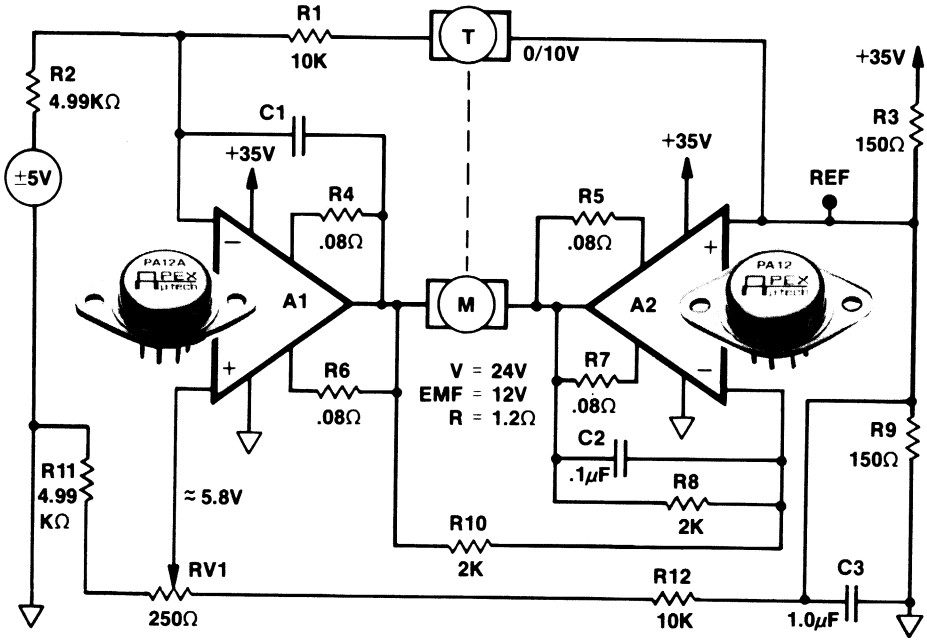



**FIGURE 1. BIDIRECTIONAL BRIDGE FOR A SINGLE SUPPLY.**

## INTRODUCTION

Two Power Op Amps configured in a bridge circuit can provide substantial performance advantages:

1. Bidirectional output with a single supply.
2. Twice the output voltage.
3. Twice the slew rate.
4. Twice the output power.
5. Half the power supply requirement.

With power op amps currently available from APEX, output voltage swings as high as 580Vpp at ±75mA and 180Vpp at ±15A can be obtained. To achieve these levels of performance, both terminals of the load must be driven and extra components are required.

## BIDIRECTIONAL DRIVE ON A SINGLE SUPPLY

Figure 1 depicts a bidirectional motor speed control using a single supply which features ground referenced bipolar input signals. A mid-supply reference created by R3 and R9 establishes the DC operating levels for A1 and A2. Inverter A2 drives the load equally in the opposite direction with respect to the output of input amplifier A1. This configuration places both load terminals at the reference voltage with a zero input condition and prevents premature saturation of either amplifier.

To understand the operation of the circuit, consider A1 as having two sets of inputs:

1. Voltage dividers from the supply voltage to establish common mode bias.
2. Actual input signal and tachometer feedback.

One sixth of any supply voltage variation will appear equally at both inputs of the amplifier. However, the common mode rejection (CMR) of the op amp will reduce its response by four orders of magnitude at low frequencies. The low pass function of C3 insures optimum rejection by keeping the common mode inputs in the low frequency spectrum. The common mode voltage (CMV) range of the amplifier sets the minimum common mode bias at the inputs of A1. The circuit shown provides a nominal of 5.8V from the supply rail (ground) which allows power supply variations to 10% below nominal.

For the actual input signal, C1, R1, R2 and A1 form an integrator (noninverting input is constant.) With the control voltage applied across R2 and the tachometer voltage applied across R1, integration forces the motor speed to be proportional to the input voltage. The value of C1 must be selected for proper damping of the total system which includes the mechanical characteristics of the drive train.

Resistors R4 through R7 set current limits to 7.5A to insure operation within the safe operating area of the amplifiers. In addition to amplifier protection, this programmability is being utilized to limit the temperature rise in the motor, thereby increasing expected life of the system. Maximum continuous load rating of the motor shown is 10A and locked rotor (stall) current is 20A. Since locked rotor ratings generally refer to abnormal conditions, the motor is being used near capacity while maintaining a comfortable safety margin for motor and drive circuit.

The key to accuracy of this circuit lies in matching the division ratios from the reference voltage to ground for both the inverting and non-inverting inputs of A1. The inverting side division ratio is effected by the impedances of the control signal and tachometer. Normally, the impedance of a voltage output DAC and the winding impedance of the tachometer are negligible. This allows use of cost effective 1% resistors and requires only trimpot RV1 to provide precision adjustment. Ratio match errors will be manifested as tachometer output errors equal to the ratio of mismatch times the reference voltage.

The second major accuracy consideration of this circuit is the voltage offset of A1. As this error will appear at the tachometer at a gain of three, the PA12A was selected for its improved specification of 3mV compared to 6mV for the regular PA12.

Changes of input voltage range, RPM range or tachometer output ratings are easily accommodated. Lowering the values of R1 and R12 (ratio match still required) will rescale smaller tachometer voltage spans or lower RPM ranges to the ±5V input level. While increased input signal levels could be rescaled the same manner, increasing R2 and R11 provides the required rescaling with the added benefit of lowering control signal drive requirements.

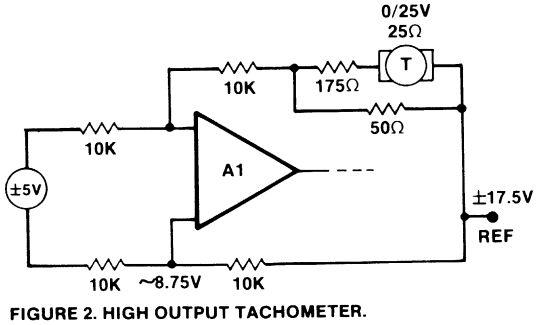



**FIGURE 2. HIGH OUTPUT TACHOMETER.**

Higher voltage tachometer voltage spans require a different approach to rescaling due to the CMV limitations at the inputs of A1. Figure 2 illustrates a technique using a 25V tachometer which will maintain adequate CMV for A1 with supply voltages down to 20V. Calculations for the divide by five network at the tachometer includes winding impedance to achieve accurate scaling to the ±5V input signal. For error budgets, this factor of five must be applied to both the ratio mismatch errors and voltage offset errors as above, (total gain for calculating offset errors will be 10).

## ELECTROSTATIC DEFLECTION

The cathode ray tube (CRT) shown in figure 3 requires 500Vpp nominal drive. Allowing for a ±5% gain error plus a 10% (of full scale) centering voltage tolerance, brings the desired deflection voltage swing to 575Vpp. Two PA84 high voltage power op amps provide this differential voltage swing. Slew rates of 400 volts per microsecond at the CRT enable the beam to traverse the face plate in less than 1.5 microseconds.

The gain of A1 is set by (R3+RV1)/R1 at 100. The circuit provides for both gain adjustment (RV1) and beam centering (RV2). For proper scaling, R4 and R6 reduce the centering control voltage of trimpot RV2 to ±250mV. C2 provides the desired low AC impedance to ground to enhance stability and eliminate noise pickup. A2 inverts the output of A1 at unity gain (set by R8/R5), to yield an overall gain of 200 for single ended input signals measured at the differential output. R9 and C4 constitute a second input to A2 with an AC gain of 100 (R9/R8). Using ground as an input has no direct signal contribution, but it does allow both amplifiers to use the phase compensation recommended at a gain of 100 (20K, 50pF), thereby achieving the large power bandwidth of 250KHz.

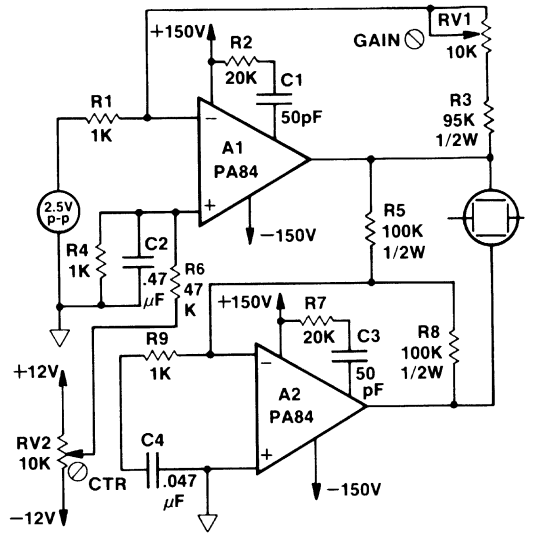



**FIGURE 3. ELECTROSTATIC DEFLECTION AMPLIFIER.**

## TRANSIMPEDANCE BRIDGE FOR MAGNETIC DEFLECTION

The circuit shown in figure 4 drives the electro-magnetic deflection yoke of a precision x-y display. Two factors constitute the design challenge of this circuit:

1. Greater than 15V drive levels are required to change current magnitude and polarity to achieve fast endpoint-to-endpoint display transition times.
2. Only ±15V power supplies are available in the system.

The bridge circuit can drive almost double the single power supply voltage, thereby eliminating the need of separate supplies solely for CRT deflection. The maximum transition time between any two points is 100μs for display ratings of:

Yoke inductance = 0.3mH
Full scale current = ±3.75A
DC coil resistance = 0.4 ohms

The voltage required to change the current in an inductor is proportional to current change and inductance but inversely proportional to transition time.

$V = di * L / dt$
$V = 7.5A * 0.3mH / 100\mu s = 22.5V$

The APEX low voltage power op amp PA02 is an ideal choice for this circuit due to its high slew rate and ability to drive the load close to the supply rail. The average output voltage swing of the circuit during the beam transition time will be greater than 26V. The configuration shown in figure 4 utilizes current sense resistor R8 to implement a voltage controlled current source for A1 while A2 functions as an inverter to double the voltage drive to the load.

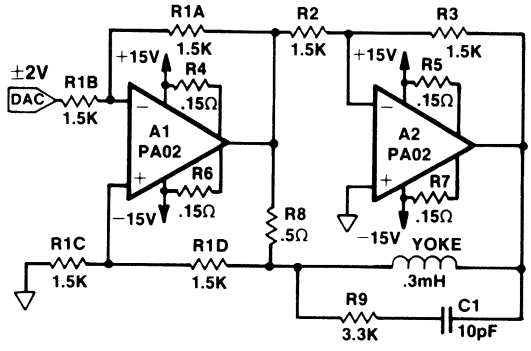



**FIGURE 4. ELECTROMAGNETIC DEFLECTION AMPLIFIER.**

In detail, the differential input configuration of A1 and R1A through R1D feeds back the output voltage of A1 as a common mode signal. In this manner, the amplifier CMR and divider ratios maintain a transimpedance function by removing the output voltage of A1 from a first order calculation of performance. Since R1A/R1B and R1C/R1D must divide this output voltage equally for both amplifier inputs, these resistors form a precision resistor network with initial matching and temperature tracking of the divider ratios. Mismatch errors can be modeled as control voltage errors equal to the percent of mismatch times the output voltage of A1. The voltage proportional to output current developed by R8 is fed back as a differential signal for comparision with the input voltage.

As the current to voltage phase relationship of the inductive load changes with frequency, the conversion function of R8 introduces phase shift up to 90° into the feedback circuit. At high frequencies, it is possible for the sum of the inductive phase shift plus the amplifier phase shift to equal 180 degrees while the amplifier still has a gain of unity. The series RC damping network placed in parallel with the inductive load reduces its phase shift and thereby eliminates the potential for oscillations.

## EFFICIENT USE OF POWER SUPPLIES

To illustrate the advantages of the bridge circuit, figures 5 and 6 show two high performance audio amplifier designs with equal output power but substantially different supply requirements. In the circuit of figure 5, the instantaneous load current will appear on only one supply rail. This means each supply rail must support the total wattage requirement and utilization is only 50% at peak outputs. In contrast, the equal and opposite drive characteristic of the bridge circuit shown in figure 6 loads both positive and negative supply rails equally during each half cycle of the signal. This improved utilization reduces size, weight and cost of the power supply for the circuit in figure 6 even though input and output power ratings are essentially equal.

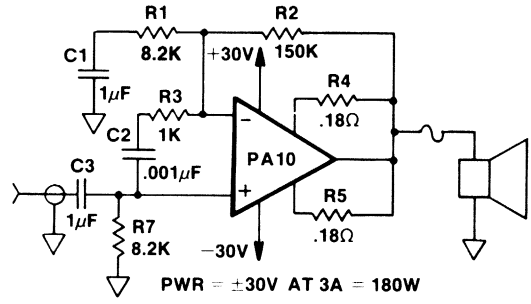



**FIGURE 5. STANDARD AUDIO AMPLIFIER.**

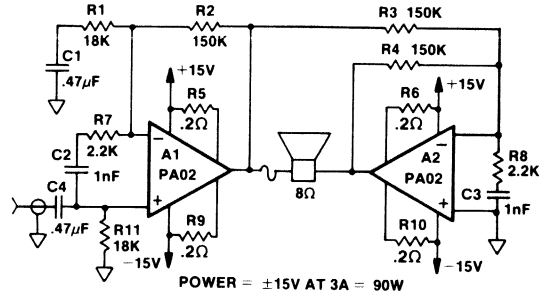



**FIGURE 6. BRIDGE AUDIO AMPLIFIER.**

## CONCLUSION

Bridge circuits can make the difference when performance requirements exceed voltage limitations of either the available power supplies or the power op amps. The input section of these circuits consists of a standard amplifier circuit for driving a single ended load. The added amplifier serves merely as an inverter. It doubles drive voltage by providing an equal and opposite output, thereby making the output fully differential. The performance increases usually outweigh the increased cost and complexity.

## SAVE HOURS OF VALUABLE TIME

This applications note is intended to save you hours (maybe days) of hard work and avoid many frustrating experiences with power circuits. It guides you through your project and points out the common pitfalls in designing and testing power operational amplifier circuits. Many of these pitfalls are theoretically predictable. The majority have been identified in APEX Applications Hotline discussions of actual circuits and range from higher than expected errors to total destruction of the amplifier.

## ELECTROSTATIC PROTECTION

In the spring and early summertime, many Arizonans become paranoid of electrostatic discharges (ESD). A walk across carpeting followed by a ¼" blue streak as one reaches for the light switch is a sign of kilovolt charges. Unless you live in a swamp, small geometry transistors used for op amp input stages are vulnerable to ESD. ESD damage causes a wide range of effects from increased voltage offsets or bias currents to total destruction. APEX products are shipped in antistatic foam to help prevent damage. Do not remove amplifiers from the foam for storage or stocking. Assembly procedures should require operators to use static straps. Be sure you touch the actual circuit ground and amplifier case with your hand prior to making contact between the amplifier pins and the circuit.

## READ THIS BEFORE YOU APPLY POWER

In the design/prototyping phase of an application many dangers exist which will be eliminated by the time it is ready for production. Pins may be wired in reverse order, connections may be missing or test probes may cause inadvertent momentary shorts. All of these can destroy power amplifiers or other components in short order. Two procedures can be employed to substantially reduce these dangers:

1. Set power supplies to minimum operating levels allowed by the data sheet.
2. Set initial current limit levels to very low levels (2.2 ohms for high current models and 47 ohms for high voltage models). Resist the temptation to use the variable current limit feature of your lab supply. It is much safer to install the initial set of resistors. Even if average power dissipation is well controlled, you must operate within the safe operating area shown on the data sheet to avoid second breakdown of bipolar output stages. This mode of destruction results from simultaneous application of high current and high voltage to the conducting transistor. While each value may be within its maximum rating, a current crowding effect in the base region due to the fields generated by the voltage can destroy the device instantaneously. A low current limit on a commercial lab supply does not afford protection due to the surge current available from the output filter capacitors.
   With low voltage applied and reduced current limits in place, the basic function of the circuit can be verified. Once the circuit is operating as desired, raise the current limit and check worst case operating conditions (i.e. motor reversal, square wave drive of reactive loads or the one half supply voltage point at the output for resistive loads). Only then should you gradually raise the supply voltages to the maximum while checking worst case operation. This procedure not only saves many failures but it also helps to pinpoint problems to specific supply voltages and power levels.

Furthermore, it is suggested to use the largest possible heatsink for your prototype work. This precaution provides the best chance to make thermal measurements on the case of the amplifier during worst case loading conditions without premature failures from thermal overload. Once you verify your calculations you can go back to the smaller heatsink you want to use.

## ABOUT CONTACTS AND SWITCHING

As you probably know, connection and disconnection of circuit components and leads should be made only with the circuit de-energized. Avoid all mechanical switches or relays in the high current branches of the power op amp. Unless the entire circuit is de-energized prior to switching, opening these contacts will create inductive kickback spikes because of the instantaneous change of current. The shorter the wires, the faster the risetime of these spikes. Amplitudes often reach several hundred volts, resulting in the immediate destruction of the amplifier. When relays or switch contacts must be used, protect the amplifier with zener diodes and capacitors at all nodes switched plus the supply pins.

These zener diodes at the supply pins may be required even though the power amplifier contains internal diodes to protect the output stages from inductive kickback. As the energy stored in the load is coupled to the power supply through these protection diodes, the power supply must absorb this transient which rises very fast. If the high frequency impedance of the power supply is too high to limit voltage transients to the absolute maximum rating of the amplifier, the short term overvoltage condition will cause the amplifier to break down.

Due to inductive kickback or slow operation, the mechanical switching of feedback elements also causes failures; particularly in circuits featuring high voltage amplifiers. Models without input protection have definite limits and models with protected inputs require limiting input risetimes to less than 1V/ns. Fig. 1A shows a simple gain select method which points out one possible problem with an unprotected input. Since the amplifier's full scale transition time (slew rate = 30V/$\mu$s) is faster than the typical relay switching time (milliseconds), the PA08 output may approach 150V while the relay is still switching. Because the 100k feedback resistor has completely discharged its associated rolloff capacitor, the relay will connect 150V directly to the input destroying the amplifier. Fig. 1B shows a protection network to prevent such damage. The diodes should be high speed devices such as 1N4148 and the series impedance should limit instantaneous current to a maximum of 150mA.

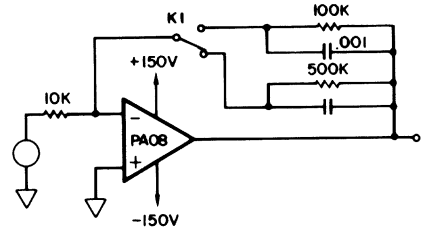



**FIG. 1A**

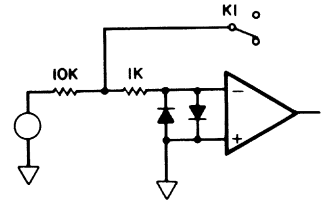



**FIG. 1B**

## USING HEATSINKS CORRECTLY

When mounting amplifiers to heatsinks, do not use insulating washers! Direct mounting with thermal joint compound results in a thermal resistance of approximately 0.2°C/watt for the TO-3 package while the use of insulating washers usually increases this figure to 0.8°C/watt. Since the cases of APEX amplifiers are isolated, inclusion of the washer raises operating temperature and lowers reliability. Refer to the APEX heatsink data sheet for hardware recommendations and the effects of junction temperature on reliability.

When mounting power op amps to a heatsink which does not have a predrilled hole pattern, drill #45 holes for each of the eight pins of the TO-3 package. Do not drill a single large hole for all the pins! Nearly all heat is produced inside the pin circle. Single hole mounting dictates a long thermal path through the steel header and between the pins of the package. Because steel is not a good thermal conductor, the amplifier will overheat even on an oversized heatsink. Short term loss of operation, blistered fingers, and total destruction of amplifiers have all been reported when using single hole heatsinks.

Due to the dimensional tolerances of the TO-3 package extreme care must be taken not to let the pins touch the heatsink inside the holes. Do not count on the anodization for insulation. Sleeve at least two pins of the amplifier if you are using a socket or printed circuit board. If you are wiring directly to the pins it is best to sleeve all pins.

## CHECK STABILITY

Amplifiers that become oscillators dissipate more power and are not reliable. If the frequency of oscillation is higher than the circuit bandwidth requirement, reactive elements of the load shift the phase. This tends to increase internal power dissipation beyond what is normally expected. Furthermore, the high power signals radiate and will interfere with communication, control, and process operations. Don't invite an FCC investigation!

Applications Note 1, "General Operating Consideration," discusses several techniques to maintain a stable circuit. A review of these suggestions can solve almost any problem. The following is a list of the most common instability situations reported:

1. Ungrounded cases cause oscillation, especially with faster amplifiers. The cases of all Apex amplifiers are isolated to provide mounting flexibility. The case is in close proximity to all the internal nodes of the amplifier and can act as an antenna. Providing a connection to ground prevents noise pickup, cross coupling or positive feedback leading to oscillations.
2. A standard inverting circuit includes an impedance matching resistor in series with the noninverting input to take advantage of the improved input offset current specification. The high impedance input becomes an antenna receiving positive feedback causing oscillation. Calculate the errors without using the resistor (some amplifiers have equal bias and offset currents negating the effect of the resistor). If the resistor is required, bypass it with a ceramic capacitor of at least 10nF.
3. Large electrolytic or tantalum capacitors are installed close to the amplifier pins as recommended but small ceramic bypass capacitors are omitted. The circuit may oscillate because the high frequency impedance of the large capacitors is not low enough to decouple the power supplies.
4. A prototype circuit is checked out and approved. A printed circuit board is built and all modes of operation test OK. A step and repeat technique then uses this same artwork to generate a multiple amplifier board. When tested, every amplifier on the multiple board oscillates. Cross coupling through the supplies and radiation is a major problem in multiple amplifier circuits. Use lots of bypass capacitors, ground the case and include an input RC network as shown in Applications Note 1 if possible.

## POWER SUPPLIES CAN BE A PROBLEM

Power op amps often require additional high voltage supplies. The additional supplies may be turned on sequentially or unpredictably. Energizing a control circuit before the power op amp results in an input to a power op amp lacking supply voltage. This violates the maximum input voltage rating. To prevent damage to the power op amp, clamp the input voltages or limit the inupt pin current to 1mA.

If operating power op amps on unregulated supplies make sure high and low line voltages have been allowed for, as well as high voltage transients on the incoming line. Due to the high speed, these spikes will pass right through most transformers and appear across the electrolytic filter capacitors. A good line filter is the first step to a solution. Zener diodes on the DC side can offer absolute protection.

## WATCH THE CURRENT LIMIT RESISTORS

The current limit circuits on APEX amplifiers are provided to allow protection within the safe operating area (SOA). The schematic of the PA01 data sheet shows the typical circuit used. This approach is fast and provides a desirable negative temperature coefficient but does not provide a precision limit. If a precision limit is called for use an external circuit. If the external circuit reduces speed it may not protect against second breakdown. Check the SOA graph before implementing the circuit.

The current limit resistors also serve to degenerate (negative feedback) tracking errors between the $V_{BE}$ multiplier bias current and the $V_{BE}$ of the power transistors. You must use a resistor (the large the better) to program no more than the maximum rated output current of the power op amp. Using a jumper will lead to increased bias current in the output stage. This raises power and temperature, while lowering resistance to second breakdown, thereby destroying reliability.

On the other side of the coin, operating the amplifiers without current limit resistors installed (current limit pins left open) can cause failures, especially with inductive loads. This includes even a momentary open circuit while switching current limits with mechanical contacts. For the high current series power op amps, minimum programmed limits should be 20mA, while 10mA is minimum for the high voltage series. Open circuits or limits below these minimums can cause voltage breakdown of the current limit transistors (Q3 and Q5 of the PA01).

## HELP IS JUST A PHONE CALL AWAY
## (800) 421-1865

The APEX Applications Hotline provides technical support all the way through your project. In many cases, specific failure prevention can be suggested immediately. In some instances we will need the amplifier to be sent to APEX for a failure analysis. The results of the analysis can pinpoint the area of damage which then narrows down the circuit problem.

## INTRODUCTION

Closed loop Power Op Amp circuits offer distinct advantages in current control over open loop systems. Using a Power Op Amp in the conventional voltage to current conversion circuit, the negative feedback forces the coil current to stay exactly proportional to the control voltage. The resulting accuracy makes many new applications feasible. For example, by placing the nonlinear impedance of the deflection yoke inside the feedback loop, steady state positioning, which is difficult, if not impossible, to achieve with open loop circuits can easily be implemented with a Power Op Amp. In addition, sweep systems with substantially improved linearity can be designed using Power Op Amps.

Typical applications include: Heads-up displays, which require random beam positioning or E-beam lithography and other complex data displays which can achieve the needed accuracy with a Power Op Amp. What is more, the versatility and ease of use of Power Op Amps will help speed up the design process while at the same time reducing development costs. The final result will be a higher accuracy display using fewer parts exhibiting better reliability.

## HIGH RESOLUTION AND HIGH EFFICIENCY

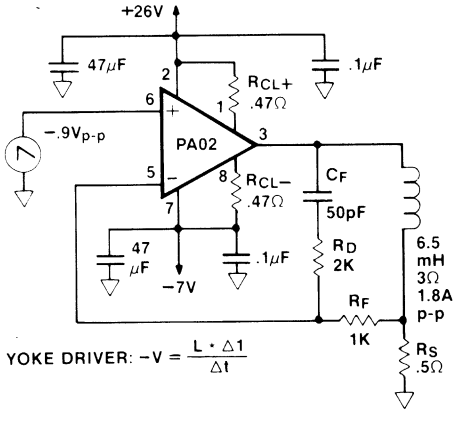



**FIGURE 1. HIGH CURRENT NON-SYMMETRICAL SUPPLY.**

The vertical deflection circuit of Figure 1 was designed to drive a high efficiency RCA CODY II tube. The PA02 was selected for this configuration because its exceptional linearity and other advantages such as high slew rate, fast settling time, low crossover distortion and low internal losses which contribute to a superior resolution display.

The key to this circuit is the sense resistor ($R_S$) which converts the yoke current to a voltage for Op Amp feedback. With the feedback applied to the inverting input and the position control voltage applied to the non-inverting input, the summing junction's virtual ground characteristic assures the voltage across $R_S$ is equal to the input voltage. Thus the highly linear control of the voltage across $R_S$ insures accurate beam positioning.

The value assigned to $R_S$ has significant impact on the performance of this circuit. All Op Amp input errors such as voltage offset, imperfect common mode rejection, offset drift, etc., will appear across the sense resistor and produce an error. This implies that $R_S$ should be as large as possible to insure that errors will be small when translated into current. Very large values of $R_S$ will reduce these errors to the point of insignificance. Unfortunately, on the downside, the voltage drive capability will be diminished and circuit power dissipation will increase because the total coil current flows through the sense resistor.

Weighing these trade-offs between errors and efficiency in the selection of $R_S$ value will produce the optimum choice for each application. The voltage drive requirements will then be defined by inductance, transition times and current. This display must operate at 50Hz or 60Hz, with retrace times of 730μs and coil currents of 2.25A p-p.

The drive voltage required to change the current in an inductor is proportional to both current change and inductance, but inversely proportional to transition time.

$$V_{DRIVE} = dI * L / * dt \quad (1)$$
$$V_{DRIVE} = 2.25A\ p\text{-}p * 6.5mH / 15ms = .98V \quad \text{(sweep)} \quad (2)$$
$$V_{DRIVE} = 2.25A\ p\text{-}p * 6.5mH / 730\mu s = 20.03 \quad \text{(retrace)} \quad (3)$$

To determine the power supply levels, add the supply-to-output differential rating of the Power Op Amp (from the Amplifier Data Sheet) and the voltage dropped across the combined values of the sense resistor plus the coil resistance, to these drive requirements to arrive at +26V and −7V as follows:

$$V_{DROP} = Ipk * (R_S + R_L) \quad (4)$$
$$V_{DROP} = 1.125Apk * (.5\Omega + 3\Omega) = 3.94V \quad (5)$$
$$V_S = V_{DRIVE} + (V_S - V_0) + V_{DROP} \quad (6)$$
$$V_S = .98V + 2V + 3.94V = 6.92V \quad \text{(sweep)} \quad (7)$$
$$V_S = 20.03V + 2V + 3.94V = 25.97V \quad \text{(retrace)} \quad (8)$$

Caution should be exercised when using nonsymmetric power supplies, as the inductive load has the potential to store energy from the higher supply. This could be initiated by an abnormal condition causing the high output voltage to remain on the yoke longer than the normal retrace time. After such an occurrence, the collapsing magnetic field would discharge the stored energy into the lower voltage supply via the inductive kickback protection diodes in the Power Op Amp. This will produce a voltage transient on the supply rail, its amplitude a function of stored energy and the transient impedance of the power supply. If this transient added to the supply voltage exceeds the rail-to-rail voltage rating of the amplifier, the result will be destructive. In such cases, a zener clamp on the amplifier output should be used.

A note of caution when using modular construction. Instruction manuals always specify, "power down first, then remove the module." However, because this doesn't always happen, protective action should be taken. The mechanical break of the connection to any inductance, coil or wire causes high voltage flyback pulses. The stored energy must be absorbed somewhere. It's much better to use the zener clamp than to risk the Op Amp.

## STABILITY CONCERNS

Since the current control capabilities of this circuit rely on feedback from the current-to-voltage conversion sense resistor, phase shift due to the inductance of the yoke will be evident in the feedback signal. Because the phase shift approaches 90° on a perfect inductor and the phase margin of an Op Amp is always less than 90°, design adaptations are required to prevent oscillation.

The network consisting of $R_D$, $R_F$ and $C_F$, serves to shift from a current feedback via $R_S$ to a direct voltage feedback at the upper frequencies. This bypasses the extra phase shift caused by the inductor. In selecting component values for this network, $R_F$ should be much larger than $R_S$, but should not exceed 1KΩ for the PA02, because the input capacitance of the Op Amp would otherwise add phase shift. Next select $R_D$ to properly dampen the circuit at the unity gain frequency. Generally, its value is a multiple of $R_F$, a safe starting value is 2 * $R_F$. Select $C_F$ for a 3db corner frequency with $R_D$ at 1/3 the unity gain frequency of the amplifier.

For the PA02's bandwidth of 4.5MHz, the $C_F$ should be 50pf.

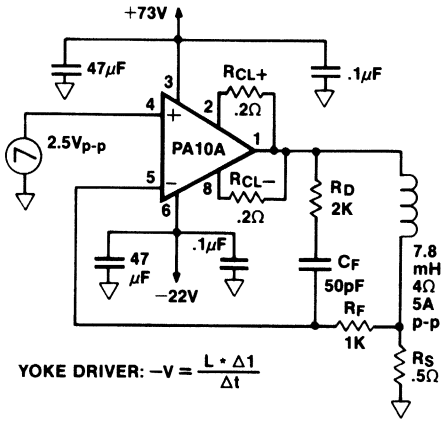



**FIGURE 2. HIGH CURRENT NON-SYMMETRICAL SUPPLY.**

For an even more powerful version of this circuit, the PA10 Power Op Amp can be used, as shown in Figure 2. With this device, a 7.8mH 4Ω coil can be driven at 5A p-p with the same timing requirements. Calculations for this design are:

| | | |
|---|---|---|
| $V_{DRIVE}$ = 5Ap-p*7.8mH/15ms = 2.6V | (sweep) | (9) |
| $V_{DRIVE}$ = 5Ap-p*7.8mH/730μs = 53.43V | (retrace) | (10) |
| $V_{DROP}$ = 2.5pkA* (.5Ω + 4Ω) = 11.25V | | (11) |
| $V_S$ = 2.6V +8V + 11.25V = 21.85V | (sweep) | (12) |
| $V_S$ = 53.43V +8V + 11.25V = 72.68V | (retrace) | (13) |

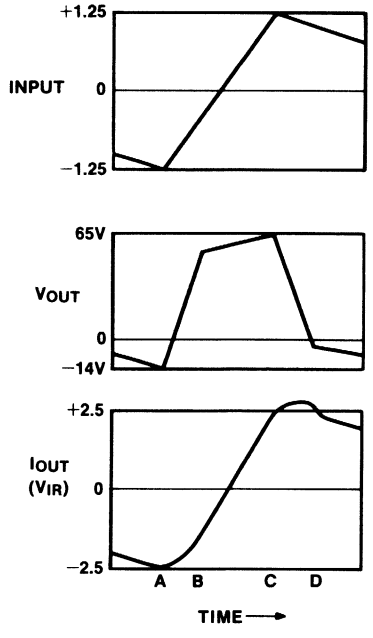



**FIGURE 3. RETRACE WAVEFORMS.**

Both of the circuits illustrated have a 730μs retrace time requirement, met easily by the Op Amp's slew rate and settling time which is substantially faster.

To better understand this and other applications, Figure 3 illustrates the output voltage waveforms generated by the Power Op Amp to obtain the desired retrace output current step for Figure 2. The waveform preceding point A is the end of the sweep waveform with a relatively slow rate of change of the current. The peak output voltage at point A equals the sum of equations 9 and 11.

Retracing begins at time A where equation 10 dictates the drive voltage required to achieve the retrace $d_i/d_t$. From time A to time B, the amplifier is running at the slew rate limit. The current in the yoke starts to track the input voltages at time B. From time B to time C, the output voltage produced is the sum of equation 3 plus the value of instantaneous IR drops (Equation 11 indicates the final value).

The abrupt slope change of the input waveform at point C again puts the amplifier in slew rate limit until the output current is proportional to input voltage according to equation 9 plus IR drops. At point D, the equation is satisfied and the amplifier will maintain the required current for the sweep portion of the waveform.

Time expansion has been used for this figure to better illustrate the slew rate and voltage swing requirements for the amplifier. During the retrace section of the waveform the amplifier has to slew the sum of drive voltage (Equations 9 and 10) twice. For the circuit of Figure 2, this amounts to 112V. With the PA10's typical slew rate of 5V per microsecond, the slew time is only 22.5 microseconds, an insignificant portion of the total retrace period. However, by understanding the voltage swing requirements, it can be seen that slew rate becomes important as the scan rates increase.

Both the PA02 used in Figure 1 and the PA10 used in Figure 2 have raised accuracy levels by placing the non-linear inductive element inside the Op Amp feedback loop. The very high gain of the Op Amp and the use of negative feedback produces superior linearity.

## RAPID TRANSITION FOR HEADS-UP DISPLAY

Heads-up displays demand swift transition between any two points on the screen. The waveforms of Figure 4 depict the input drive voltage and required current to the yoke to achieve a single fullscale step in beam position for the circuit in Figure 5. The 3V levels sustain the steady state current through the coil resistance and the sense resistors. The 29V level corresponds to the peak output voltage required for a position change.

Starting with amplifier slew rates and settling times from the data sheet, it is determined what percentage of the total transition time will be required for slewing and settling. A reasonable starting point would be to allow 50% of the total transition time.

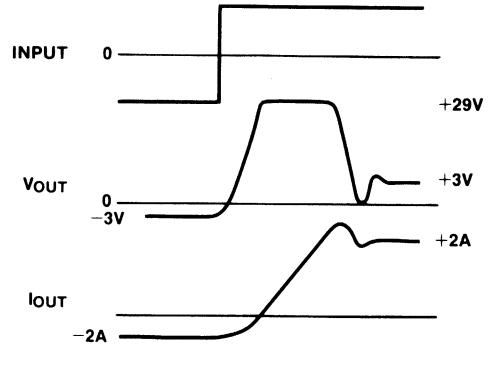



**FIGURE 4. FULL SCALE STEP FUNCTION WAVEFORMS.**

This circuit was designed for a maximum transition time of 4$\mu$s when delivering 2A Pk currents to the 13$\mu$H coil. While the fundamentals of this circuit are the same as previously detailed, there are differences due to the higher speed. To achieve rapid transitions, amplifier slew rates must be optimized. The PA09 Video Power Op Amp with external phase compensation allows this. However, close examination of poles and zeros in the feedback loop is required because reactive feedback elements force the amplifier to operate over a very wide range of gains, very high during transition but unity at steady state.

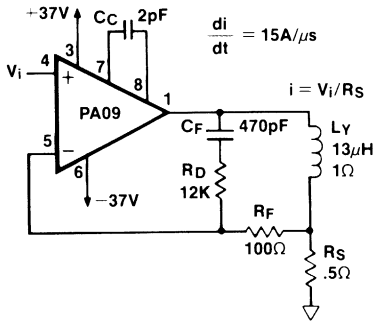



**FIGURE 5. PA09 AS DEFLECTION AMPLIFIER.**

The network of $C_F$, $R_D$ and $R_F$ set gain to approximately 100 at high frequencies. This allows phase compensation for a gain of 100 and correspondingly high slew rates. The next step, shown in Figure 6, is to plot the feedback zero of the yoke inductance and the sense resistor. Then the high frequency feedback level of the

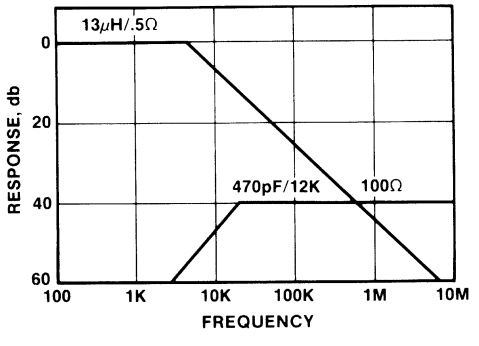



**FIGURE 6. FEEDBACK RESPONSE.**

RC network, approximately 40db, was drawn in and $C_F$ was selected to produce a pole approximately one decade below the intersection point. Figure 7 shows the PA09 open loop bode plot and the modification due to feedback effects, a slope increase below 500KHz and a shallow slope at the unity crossing point to insure stability.

If 50% of the total transition time is allowed for slewing and settling, 2$\mu$s will remain to change the yoke current with full voltage applied to the coil. Voltage requirements are calculated as follows:

$$V = di \cdot L/dt \quad (14)$$

$$V = 4A \cdot 13\mu H/2\mu s = 26V \quad (15)$$

$$V_{DROP} = 2A \cdot (.5\Omega + 1\Omega) = 3V \quad (16)$$

$$V_{DRIVE} = 26V + 3V = 29V \quad (17)$$

$$V_S = 29V + 8V = 37V \quad (18)$$

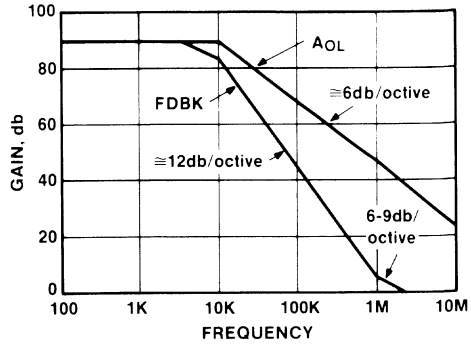



**FIGURE 7. COMPOSITE RESPONSE.**

Selection of the external phase compensation will also need to be calculated as applicable to the PA09. Component values are recommended on the Amplifier Data Sheet according to the effective gain setting of the circuit ($R_D$ to $R_F$).

With the external compensation selected, the PA09 Data Sheet indicates that the amplifier slew rate will be 400V per microsecond. For a calculated swing of 58V the required voltage slewing time is 145 nanoseconds. Adding the settling time to 0.01% of 1.2$\mu$s, the total is comfortably below the 50% allotment of 2 microseconds.

When the circuit was tested, values were further optimized for best performance. The value of $R_D$ had a considerable effect on damping of the circuit. This could be predicted because $R_D$ affects the corner frequency where the roll off slope must be flattened near the unity gain point. The value of $C_F$ was not particularly critical. However, a compensation capacitor of 2pF as opposed to the data sheet recommendation of 5pF helped to increase the slew rate without significant effects on stability.

Due to the high speed of PA09, specific precautions are recommended to insure that optimum stability and accuracy are maintained:

1. To help prevent current feedback, use single point grounding for the entire circuit or utilize a solid ground plane.
2. To insure adequate decoupling at high frequency, bypass each power supply with a tantalum capacitor of at least 10$\mu$F per ampere of load current, plus a .47$\mu$F ceramic capacitor connected in parallel. The ceramic capacitors should be connected directly between each of the two amplifier supply pins and the ground plane; the larger capacitors should be situated as close as possible.
3. Use short leads to minimize trace capacitance at the input pins. Input impedances of 500Ω or less combined with the PA09 input capacitance of approximately 6pF will maintain low phase shift and promote stability and accuracy.
4. The output leads should also be kept as short as possible. In the video frequency range, even a few inches of wire have significant inductance thereby raising the interconnection impedance and limiting the output slew rate. Also, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.
5. The amplifier case must be connected to an AC ground (signal common), even though it is isolated, for it can act as an antenna in the video frequency range and cause errors or even oscillation.

## TRANSIMPEDANCE BRIDGE FOR HIGHER DRIVE VOLTAGE

The circuit illustrated in Figure 8 drives the deflection yoke of a precision x-y display from an available ±15V supply. Only the bridge configuration can provide the high voltage drive levels required with the power supplies available. This enables the system to drive double the single amplifier output voltage. Consequently, the need for separate power supplies solely for CRT deflection is eliminated.

Figure 8 shows the current sense resistor R8 utilized to implement a differential voltage-controlled current source (transimpedance) with A1, where A2 functions as an invertor to provide an equal but opposite phase voltage drive to the load. To convert the single ended input to the differential output, the differential feedback of R1A through R1D makes the output voltage a common mode signal for A1 negating any feedback effects. In this manner, the amplifier common mode rejection and the resistive divider ratios maintain the transimpedance function (differential feedback from R8 only). Because R1A/R1B and R1C/R1D must divide the output voltage equally for both amplifier inputs a matched or precision resistor network must be used. In addition to initial matching, temperature tracking of the divider ratios is also critical. Mismatch errors are equivalent to control voltages equal to the percent of mismatch multiplied by the output voltage of A1. The series RC damping network placed in parallel with the inductive load reduces its phase shift at high frequencies, which effectively eliminates the possibility of oscillations.

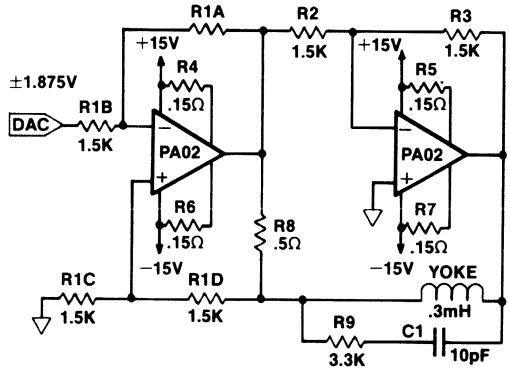



**FIGURE 8. CURRENT-OUT BRIDGE DRIVE.**

The maximum transition time between any two points is 100μs for display ratings of:

Yoke inductance = 0.3mH
Fullscale current = ±3.75A
DC coil resistance = 0.4Ω

Calculations are identical to previous examples:

$V = di^*L/dt$ (19)
$V = 7.5A^*0.3mH/100\mu s = 22.5V$ (20)
$V_{DROP} = 3.75A^* (.5\Omega + .4\Omega) = 3.375V$ (21)
$V_{DRIVE} = 22.5V + 3.375V = 25.875V$ (22)

One-half the total drive level required for the bridge circuit is provided by each amplifier, or approximately 13V of output swing per amplifier.

The APEX low voltage Power Op Amp PA02 perfectly meets the criteria for this circuit because of its high slew rate of 20V/μs and its ability to drive the load close to the supply rail. The average output voltage swing of the circuit during the beam transition time will be greater than 26V as illustrated in Figure 9.

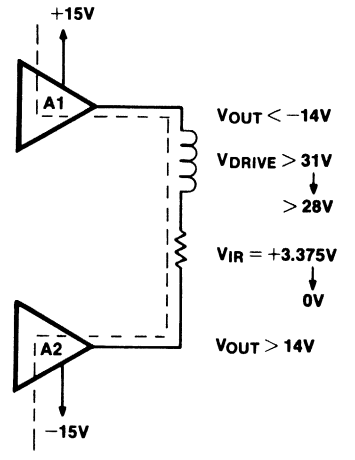



**FIGURE 9. CURRENT PATH AND VOLTAGES DURING THE FIRST 50% OF A FULL SCALE TRANSITION.**

Due to the inductive nature of the load, the direction of current flow changes only after the transition is 50% complete. This allows both amplifiers to swing to their no load saturation levels (less than one volt from the supply rail) for this time period. Furthermore, IR drops during this time period generate voltages which add to the amplifier drive. During the second half of the transition, current direction changes and the amplifier output swing decreases. However, even at 75% completion, each amplifier will still swing in excess of 13V because the current magnitude has not yet reached 2A (see data sheet).

## CONCLUSION

The capabilities of the Power Op Amp provide higher accuracy levels, the ability to position beams in any desired position and to retain a steady state position. Having both the power and signals stage in one compact package offers space/weight advantages. The lower parts count increases reliability.

Power Op amps are comparatively inexpensive and easy to use. They represent the most efficient solution to reducing development costs and decreasing design time.

# POWER OPERATIONAL AMPLIFIER APPLICATIONS NOTE 6
## APPLYING THE SUPER POWER PA03

## INTRODUCTION

The Super Power PA03 is the result of a design effort to substantially increase output power without sacrificing the high performance engineers are accustomed to when using small signal Op Amps. Thus the new building block can perform accurate and complex tasks previously reserved to modular and rack mount devices.

The major applications for the PA03 will be in single ended circuits where up to 1,000W must be delivered to the load or bridge motor servo systems delivering up to 2,000W peak. Linear motion control, magnetic deflection, programmable power supplies, and power transducer drives are typical of these applications. High power sonar, such as phased array, is another key application made possible by the accurate phase response and linearity of the class A/B output stage. Robot, motion control, and other high current applications which were previously impossible to implement with IC Power Op Amps because of power limits are now possible using the PA03 as a building block.

The most powerful TO-3 hybrid IC's currently available can dissipate up to 125W and drive loads up to 250W (APEX PA12), while available monolithic IC's can handle even less. Where peak power requirements for dynamic motor control exceed 250W, three approaches were commonly used to increase power output. (1) parallel or bridge operation of two or more Power Op Amps; (2) external booster transistors; (3) Modular or Rack Mount Power Op Amps.

While these options extend power capabilities, they can have major drawbacks in increased cost, excessive weight, and reduced reliability. Furthermore, the large size can be a cumbersome design burden. System designers need a small, reliable Power Op Amp capable of producing up to 1,000W while maintaining top notch performance. The PA03 meets this challenge!

Using the Super Power PA03 offers many advantages. With an internal power dissipation of up to 500W, the PA03's ratings top the previously most powerful Op Amp (APEX PA12) by a factor of *four*, and *one* PA03 is more cost effective and far more reliable than *four* "other" Op Amps. It's thermal tracking of internal bias components makes the PA03 much safer to use under abnormal conditions than several units in parallel. What's more, internal protection circuits insure that almost any power level not violating the 2,400W, 1ms Safe Operating Area (SOA) is safe. The amplifier will shut down upon overload, avoiding self-destruction. Internal current limiting resistors eliminate bulky, expensive milliohm external resistors which are normally required for Power Op Amps. The common collector complementary output stage allows the output to swing within 4V or the supply rail at 12A and within 6V at 30A, and has full shut-down control. This gives the designer a tool to protect sensitive loads or to use power efficiently under battery operation. By operating in class A/B, it exhibits low crossover distortion, a feature hard to implement without the inherent thermal tracking of single package construction.

An external balance control option allows the already low offset voltage to be zeroed. The PA03's high overall accuracy makes it suitable for interfacing directly to photo-diodes, to build long time period integrators, or to design 12 bit and better resolution programmable power supplies.

The Super Power PA03 is a hybrid IC housed in the innovative Power-Dip dual in-line package. It has .060 pins on .200 centers to accommodate higher currents and allows layout on the standard 0.100 grid. The Power-Dip copper header of the PA03 provides 8.5 times the thermal conductivity and three times the area of the conventional steel TO-3 package.

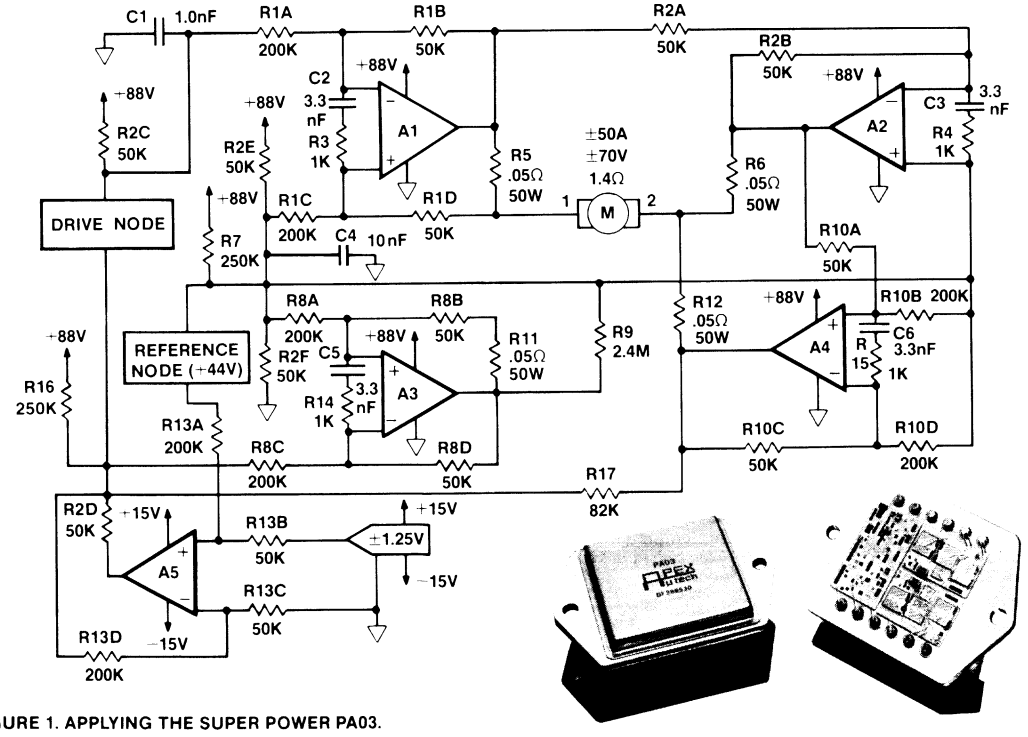



**FIGURE 1. APPLYING THE SUPER POWER PA03.**

## A SUPER POWER TORQUE DRIVE

The parallel bridge circuit in Figure 1 is shown to demonstrate several possible power enhancement techniques in one application. It operates in the transimpedance mode to drive the torque motor. This allows the D to A converter (DAC) to be programmed directly for delivered torque, since motor torque is directly proportional to armature current. The bridge uses an economic and efficient single output power supply and doubles delivered power over that of the single amplifier. The parallel combination shown here to illustrate further power enhancement doubles power levels again by increasing the current drive capability. Delete A3 and A4 and associated components if this option is not required.

Looking at the bridge configuration first, A2 and A4 invert the output of A1 and A3 with respect to the mid-supply reference node. Therefore, A2 and A4 drive the load equal to A1 and A3 in the opposite direction about the mid-supply reference point. The mid-supply node assures that neither amplifier saturates prematurely. Figure 2 shows the actual output voltages of A1/A3 and A2/A4 when delivering full scale output currents to the torque motor.

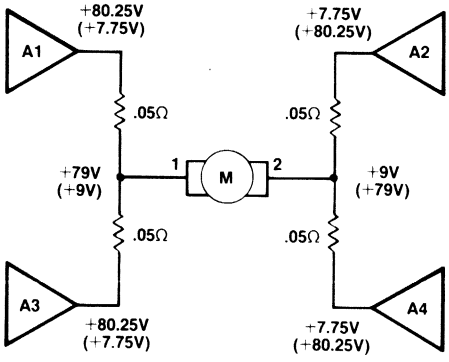



**FIGURE 2. FULL SCALE DRIVE VOLTAGES.**

A5 configured as a level shifter at a gain of 4, takes the 1.25V input from the DAC and swings the drive node to ±5V with respect to the reference node. A1 and A3 each amplify this differential 5V signal to a ±25A output level driving terminal 1 of the motor. A4 is a unity gain follower of the A2 output voltage. Since A2 and A4 have equal output voltages and equal current control resistors, they share equally the total 50A current.

The very low bias current of the PA03 FET input stage makes it possible to keep power dissipation low by using relatively large value precision resistors. This not only minimizes temperature variations in the resistive networks but also reduces power dissipation in A5. Current balancing for both the reference and drive nodes is used to prevent level shifting of the high impedance nodes as a function of drive voltage. This is an easy task because of the symmetric drive levels with respect to the reference node.

Figure 3 shows a breakdown of the currents associated with the reference node. R2E and R2F form the basic voltage divider. At a zero drive level, the current through R13A and B will match the current through R7. The voltages applied to R1, 8, 9, 10, will all be zero with respect to the 44V reference so the circuit is balanced. The voltages shown correspond to full scale drive level. R7 roughly balances the current through R13A and B to the ±1.25V DAC input. R10A, B, C, and D current will nearly match the currents of R1C and D plus R8A and B. The differences encountered so far total 15 microamps, which is provided by R9 to insure the reference node remains at 44V.

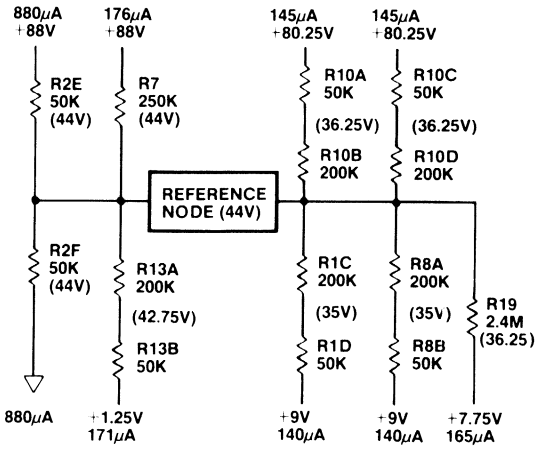



**FIGURE 3. CURRENT BALANCING OF THE REFERENCE NODE.**

Figure 4 illustrates currents associated with the drive node where R2C and D form the basic voltage divider. At zero drive, no voltage is applied to R17, R1, and R8 and the output of A5 will be zero and the drive node voltage will be 44 volts. This means currents of R2C and D balance. The currents in R16 balance the currents of R13C and D and the remaining resistor currents are zero. For a full scale input of +1.25V, A5 will drive to approximately +10V. The currents through R16 and R13C and D are no longer balanced because the drive node voltage has risen to 49V. The currents through R1A and B plus R8C and D make the node even less balanced. R17 was selected to slightly over componsate the current imbalance. Since the differential circuit of A5 controls drive node voltage, its nominal swing will be a 9.44V, correcting the overall current imbalance of 12μA. Thus the overcompensation of R17 insures A5 will not be required to swing beyond it rated 10V due to component tolerances.

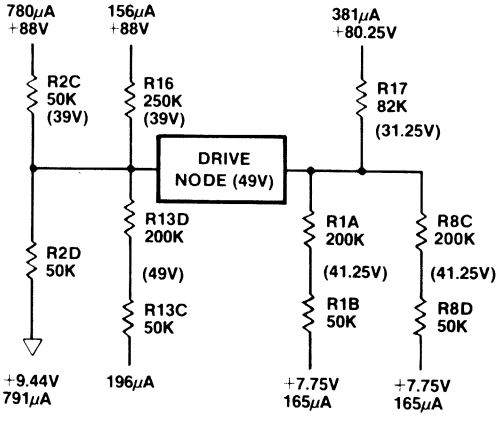



**FIGURE 4. CURRENT BALANCING OF THE DRIVE NODE.**

There are a lot of resistor networks in the circuit, but each has a critical task. The ratios are most important to insure gain accuracy. In addition, ratio matching provides common mode rejection and differential voltage amplification. Specifically, the R13 quad around A5 sets drive node swing to ±5V with respect to the reference voltage even though the reference changes with supply variations. Similarly, the R1 quad and the R8 quad set the full scale voltage across sense resistors R5 and R11 at ±1.25V.

The ±35V output swings across the impedance of the torque motor are rejected as a common mode signal to maintain the programmed voltage to current transfer function. Thus, impedance variations of the motor winding and the associated connections do not affect accuracy. R10 fixes the gain of A4 to unity while keeping its input pins about 4V closer to the reference than the amplifier's output voltage. With the output swinging to within nearly 7V of the supply rails, the common mode voltage requirement of $\pm V_S$ - 10V is satisfied.

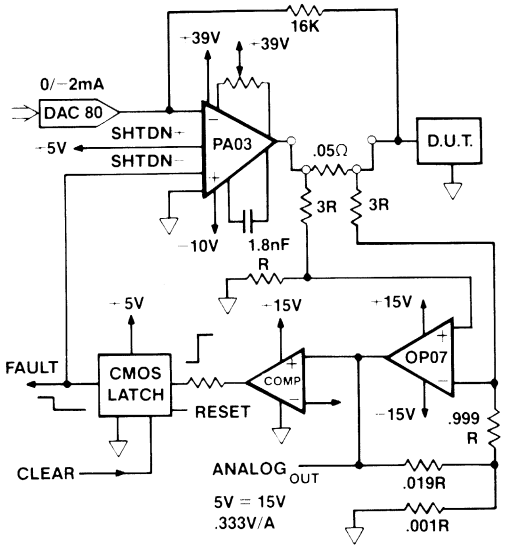



**FIGURE 5. HI-POWER PROGRAMMABLE POWER SUPPLY APPLICATION.**

## A PROGRAMMABLE POWER SUPPLY USING THE PA03

Figure 5 shows the PA03 in a simple, reliable programmable power supply which utilizes the PA03's shutdown features. It requires little calibration because the current to voltage conversion of the D to A converter output is done by the Power Op Amp itself, and the 12 bit DAC80 provides accuracy levels high enough to eliminate the need for adjustments.

The programmable power supply is designed to test DC-to-DC converter modules drawing up to 15A. The majority of tests are performed at 28V. High and low limits of 18.5V and 32V will be applied for 500ms. The outputs must be accurate to within 0.5% and survive an occasional short circuit to ground.

The OP07 differential amplifier circuit senses the D.U.T. current on the four-terminal shunt resistor, and provides a signal of 0.333V/A to the comparator. The comparator will trip at a current of 18A, setting the latch, and the latch then shuts down the PA03 until the fault is cleared and the latch is reset. This safety circuit limits arcing hazards in the test socket.

The feedback resistor of 16kΩ yields the required 32V full-scale output when the DAC output is 2mA. The 0.05Ω current sense resistor develops a 0.75V signal at the full-scale output current of 15A. This amplitude is a compromise between monitoring the current accurately without imposing an excessively high power rating on the sense resistor. However, the sense resistor still must be mounted on a heatsink due to 11.25W dissipation at 15A and the possible 88W at the built-in maximum current limit of 42A.

To derive the power supply voltage needed, the 0.75V drop on the sense resistor must be added to the headroom (supply-to-output differential) required by the Op Amp. From the PA03 specifications, a drop of 7V at 30A and 5V at 12A, a maximum drop of 6V at 15A can safely be assumed. Selecting a positive voltage of 39V leaves a margin of 0.25V. Without remote sensing, such a conservative approach is best due to potential IR drops in the high current leads. For the negative supply, a minimum operating voltage of 10V is required to satisfy the input common mode voltage specifications.

Four power levels must be examined to determine the worst case maximum power dissipation of the Power Op Amp. The first three are the output voltage levels for the devices under test at the maximum current of 15A. Calculating all three shows the 18.5V output to be the worst case scenario. The 18.5V output plus the 0.75V drop across the sense resistor leaves a voltage of 19.75V across the output stage of the PA03. At 15A, this produces an internal power dissipation (including quiescent power of 9.8W) of 306W and a junction to case temperature rise of 92°C (PA03=0.3 C/W).

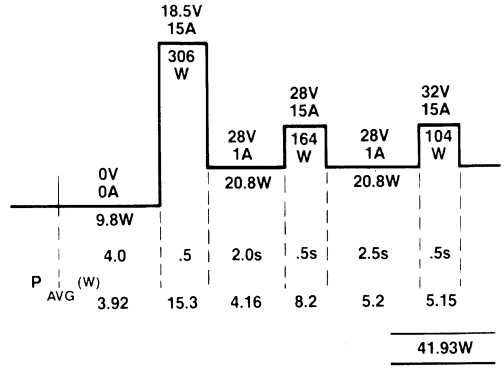



**FIGURE 6. PROGRAMMABLE POWER SUPPLY INTERNAL POWER DISSIPATION.**

Because the worst case power demand exists only for 500ms, an examination of average power and thermal time constants will help to reduce the heatsink size. Figure 6 shows the general test plan and the specific testing sequence with the resulting power dissipation levels demanded of the PA03. The 32V output level requires 103.6W (39V supply less 32V output and 0.75V across the sense resistor times 15A plus 9.8W of quiescent power) for 500ms. The 28V level amounts to 163.6W (39V supply less 28V output and 0.75V across the sense resistor times 15A plus 9.8W of quiescent power) for another 500ms.

For the balance of the test of 4.5s the maximum current of 1A amounts to 20.8W. During the minimum removal/insertiion time of 4s the power dissipation is only the quiescent power of 9.8W. This means the average power dissipated is only 41.9W. With a heatsink that has a thermal time constant of ten seconds, the highest peak (306W for 500ms) amounts to 5% of the time constant, or 4.9% of the rise, for 306W continuously. Adding this spike equivalent of 15W to the 41.9W average will bring the peak short term equivalent power to 57.23W (though this peak could vary slightly depending upon the exact timing).

If, for reliability, a peak junction temperature of 150°C is selected, and a maximum ambient temperature of 38°C is assumed, the allowable temperature rise of the heatsink is 18°C (150°C - 38°C - 92°C). At a peak short term equivalent of 52.2W, this requires a heatsink rated at 0.35°C/W. The APEX HS06 (0.6°C/W free air) with a forced air velocity of 500 ft/min. can provide the required rating.

In this application, if abnormal situations arise due to faulty timing or defective test units, short term operation at the 306W level will not destroy the PA03 because the thermal shutdown will limit the temperature rise. The worst case would be a short in the test socket which could push the PA03 to a maximum current limit of 42A. At this current, the sense resistor ($R_S$) would drop 2.1V leaving 36.9V across the PA03. These current and voltage levels (1.55KW) are well within the PA03's 1ms secondary breakdown line of the SOA curve. Therefore, the fast response of the PA03's thermal shutdown circuit will protect the Power Op Amp for the time required to eliminate the short.

## REMOTE SITE MOON BOUNCE ANTENNA MOTOR DRIVE

Power conservation is essential for solar powered data gathering, while a considerable amount of motive force is required for positioning a forty foot dish antenna.

With a 3° beam angle and a position accuracy of 0.5°, the lunar angular velocity of 14.4°/Hr allows a position update only once per minute. The PA03's shutdown control used for intermittant operation combined with a worm gear drive to hold position during shutdown periods, facilitates an energy efficient positioning system.

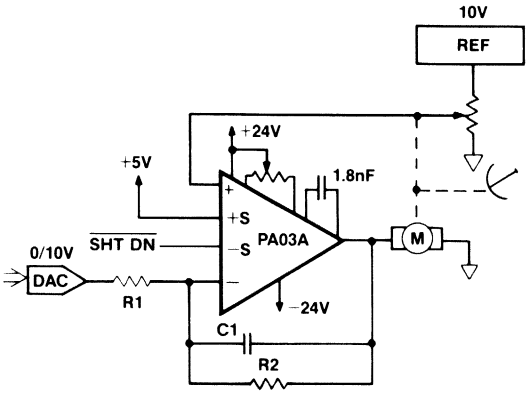



**FIGURE 7. REMOTE SITE MOON BOUNCE APPLICATION.**

The D to A Converter in Figure 7 converts position data to a voltage which is fed to the inverting input of the PA03 configured as an integrator by feedback capacitor C1 and input resistor R1. The precision reference and potentiometer apply a feedback voltage equivalent to actual position to the non-inverting input. The PA03 drives the motor with the integrated difference between the desired and actual positions; R2 acts as a damping element limiting the integration time constant to minimize overshoot.

The shutdown control is released for six seconds after each position update, which allows the PA03 sufficient time to position the antenna and reduces the standby power to 2W for fifty-four seconds or 90% of the time.

The normal current requirement of the motor is 8A, but under high wind conditions up to 17A may be drawn. In this application, the amplifier output will be decaying pulse driving the motor to a new position once a minute. Because the amplifier is at maximum output (saturated) most of the time, the power dissipation at the full output voltage is the appropriate level to calculate.

At 17A the PA03 will drive to within 5.5V of the supply voltage (rail), dissipation 93.5W. The quiescent current of 0.2A times the total supply voltage of 48V adds another 9.6W for a total of 103.1W dissipated in the amplifier. At the maximum ambient temperature of 45° and a maximum junction temperature of 140°C, the allowable rise is 95°, which requires a thermal resistance for the heatsink of: $\Theta_{HS} = 95/103.1 - 0.3 = 0.62°/W$. The APEX HS06 meets this criteria.

Under normal low wind conditions, the peak battery drain will be 201.6W. However, due to the 10% maximum duty cycle and the power-saving shutdown feature of the PA03, the average power consumption will be only:

$$P_{AV} = 0.1\ (24 \cdot 8 + 48 \cdot 0.2) + 0.9\ (48 \cdot 0.040) = 22W$$

To further reduce standby power to 2W, the shutdown feature can be activated only when communications are required.

## USING THE PA03 IN YOUR APPLICATION

To achieve maximum efficiency, the power supply voltage should be selected for the minimum voltage necessary to produce the required output.

For example, to obtain a ±45V output at 12A, add the supply-to-output differential as specified on the Data Sheet (±5V) to produce ±50V.

Dual supplies may be as high as +75V and non-symmetric or single supply operation is permitted as long as the total rail-to-rail voltage doesn't exceed 150V. Input voltages must always be at least 10V less than the power supply voltages due to the common mode voltage specification being supply voltage minus 10V.

Because of the greater power levels involved, the thermal path to remove the heat from the amplifier is of great importance to the successful application of the PA03. A 1°C/W rated heatsink may be suitable to remove 20-50W, but it is insufficient to handle 500W. For the PA03, a heatsink with a thermal resistance on the order of 0.1°W is often required: very large sufaces, forced air cooling, or even water cooling. Fortunately, if insufficient heatsinking is provided, the unique safety circuits of the PA03 will generally result in thermal shutdown rather than destruction. Destructive power levels are so high that in most applications they need not be of any concern.

As with all high current Power Op Amps, precautions must be taken to avoid current feedback due to voltage drops in the wiring or electromagnetic radiation. This is especially true when using the PA03 because of its higher current rating. The wiring for all supply and output leads must be done with wire equivalent to 12 gauge or thicker, as the PA03 has a higher current capacity than most branch circuits in residential wiring.

To avoid feedback through the power supplies, they must be bypassed with a ceramic capacitor of 0.47μF or greater, in parallel with a 10μF per ampere of peak output current (up to 300μF), mounted not more than 1.5 inches from the supply lines.

Even when using excellent bypassing components, good layout techniques and quality power supplies, large rectified currents in the supplies can easily cause substantial AC ripple. Ripple must be considered as a possible source of error. Positive feedback can also occur if the power supply also powers other circuit elements.

## WATCH THE POWER DISSIPATION

The Internal Power Dissipation (P) in a DC circuit is:

$$P = (V_S - V_O)\ I_O + (|+V_S|+|-V_S|)\ I_Q$$

where $I_O$: OUTPUT CURRENT

$I_Q$: QUIESCENT CURRENT

$V_O$: OUTPUT VOLTAGE

$V_S$: SUPPLY VOLTAGE

Errors often arise in the calculation if the wrong supply voltage is used. The voltage ($V_S$) must be the one at the supply pin sinking or sourcing the current. Incorrect selection of the worst case conditions (short to ground or supplies) can also create errors.

When driving reactive loads, due to the phase shift between output voltage and current, the Power Dissipation may be several times higher than the equivalent resistive loads. These have a totally different, but equally simple approach that can be used to obtain the correct Power Dissipation (P):

$$P = P_I - P_O$$

where $P_I$ = POWER DRAWN FROM THE POWER SUPPLY

$P_O$ = POWER DELIVERED TO THE LOAD

Keep in mind using purely reactive loads means that all power drawn from the supplies is dissipated in the amplifier.

## JUNCTION TEMPERATURES

The absolute maximum power dissipation of the PA03 is 500W and was derived using the industry standard derating procedure, which assumes operation at maximum junction temperatures (175°C) with the case at 25°C.

With the power dissipation and the maximum ambient temperature ($T_A$) of the application known, the operating temperatures of both case ($T_C$) and junction ($T_J$) of the power transistors can be determined:

$$T_C = T_A + P \cdot \Theta_{HS}$$

where $\Theta_{HS}$ = THERMAL RESISTANCE FROM THE HEATSINK MOUNTING SURFACE TO AMBIENT AIR

$\Theta_{JS}$ = INTERNAL THERMAL RESISTANCE, JUNCTION TO CASE

Apply this to the PA03 by following these steps:

1. Calculate the maximum Internal Power Dissipation (P).
2. Determine the maximum Junction Temperature allowable to achieve the desired reliability of the PA03. This must be less than 175°C. APEX recommends 150°C or less.
3. Calculate $T_J - T_A$, the allowable rise of the junction temperature above the maximum ambient temperature.
4. Calculate the required thermal resistance of the heatsink: $\Theta_{HS} = (T_J - T_A)/P - \Theta_{JC}$.

For example, in a circuit dissipating 300W at an ambient temperature of 30°C and the junction temperature not to exceed 150°C:

$$\Theta_{HS} = (150 - 30)/300 - 0.3 = 0.1\ ^\circ C/W$$

## HOW THE PA03 WORKS

The circuit diagram shown in Figure 8 shows that the input section of the PA03 is similar to most APEX FET — Input hybrid power op amps. Q21, D1 and D4 form voltage references to bias both input and output stages of the amplifier. Q31 is the current source for the input stage which consists of Q20A and B the FET input pair, Q17 and Q18 the cascode transistors, and Q2 and Q3 the half dynamic load. The current through Q5 sets the operating voltage (source-drain) for the FET input pair. Q12 acts as an impedance buffer between the high output impedance of the input stage and Q6, the output driver.

The collector load of output driver Q6 consists of current source, Q29, and the output stage consisting of Q16, Q9, Q24 and Q26. The common collector configuration of Q9 and Q26 enable the PA03 output to swing close the supply rails. Inverters Q16 and Q24 form local feedback networks which cause the output stage to be linear like an emitter follower with very high input impedance. The $V_{BE}$ multiplier Q19, provides DC bias for the output transistors via Q16 and Q24 and is thermally coupled to the power dissipating transistors in the output stage. In addition, the $V_{BE}$ multiplier utilizes thermistors to fine tune the temperature stability of the quiescent current through output transistors Q9 and Q26. This class A-B stage provides low crossover distortion as well as stability of the quiescent current over the full temperature range.

D2 and D3 are high speed diodes which protect the output stage from inductive kickback by bypassing it into the supply rails. The 18.6 milliohm emitter resistors of Q9 and Q26 sense the output current of the amplifier. Currents in excess of 35 amps will develop .65 volts thereby turning on Q1 or Q34. In turn these transistors rob the base drive from Q6 or Q29, thus limiting the output currents to 35 A. Q4 and Q32 are the sensors for the innovative SOA protection of the PA03. These two transistors are mounted directly on top of power transistors Q9 and Q26, eliminating thermal gradients and minimizing the response time to temperature changes in the output transistor junctions. The emitters of the sensors are connected to Q7 and Q30 which act as level translators to turn on current limit transistors Q1 and Q34, respectively. The complementary pair Q14 and Q22 activate the shut down of the PA03. While common mode voltage is rejected, differential voltages applied between these two transistors turn on the current limit circuit consisting of Q1 and Q34, thereby shutting down the entire output stage. In this mode the output pins appear as a high impedance to the load. Figure 9 illustrates the physical arrangements to achieve fast and reliable thermal shut down.

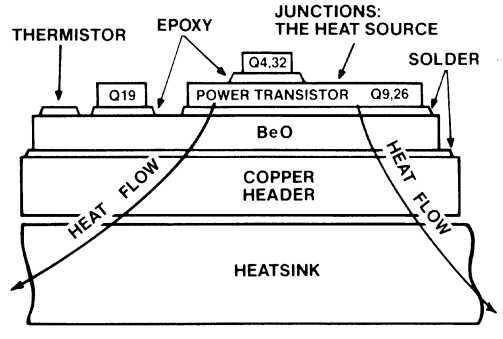



**FIGURE 9. THERMO-MECHANICAL DESIGN.**

## CONCLUSION

The PA03 is an versatile new building block which eases many design tasks and overcomes size and weight barriers which previously prevented implementation of linear power controls in limited space. The giant step up in power levels, improved protection circuits and high performance small signal characteristics make the PA03 a very cost effective innovation.

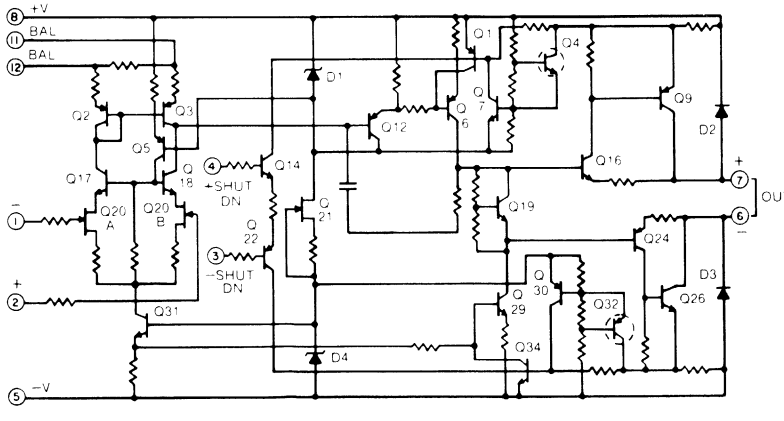



**FIGURE 8. PA03 EQUIVALENT SCHEMATIC.**

The Programmable Power Supply (PPS) is not only a key element in automated test equipment but is also used in fields as diverse as industrial controls, scientific research and vehicular controls. When coupled to a computer, it bridges the gap from the software to the control task at hand. This application note examines the basic operation of the PPS, the multitude of possible configurations and the key accuracy considerations.

## VOLTAGE OUTPUT VERSIONS

The most basic and often most accurate version of the PPS requires only a current output Digital to Analog Converter (DAC), a Power Op Amp and a feedback resistor as illustrated in Figure 1. According to op amp theory, the voltage at the inverting input (summing junction) will be zero and op amp input current will be zero. As a result, all current from the DAC flows through the feedback resistor $R_F$. Ohm's law then causes the circuit to provide a precise output voltage as a function of DAC output current.

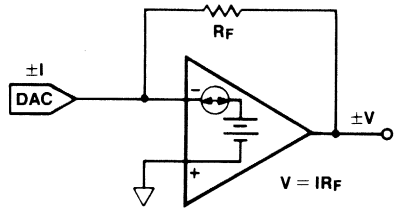



**FIGURE 1. I TO V CONVERSION.**

Given a perfect DAC and feedback resistor, only two op amp parameters contribute significantly to the ouptut voltage errors. These are voltage offset ($V_{OS}$) modeled by the battery and bias current ($I_B$) represented by the current source. Due to the high output impedance of the current output DAC in relation to $R_F$, $V_{OS}$ errors appear at the output without gain.

For a 10V output and op amp offset of 5mV, this error contributes only 0.05%. For a 100V output, a 0.5mV offset contributes an error of only 5 ppm. Clearly, the DAC can easily be the major error source.

Op amp bias currents add to the DAC output current. The majority of available DAC's have full scale currents of ±1mA or 0/2mA. Most of today's bipolar input Power Op Amps feature bias currents of less than 50nA. This results in errors of only 25 ppm maximum of the full scale range (FSR). FET input bias currents at 25°C are seldom over 100pA and are specified as low as 10pA. These errors translate to 0.05 ppm and 0.005 ppm. Since FET bias currents are generally characterized as doubling every 10°C, the bias current of the two examples could become 100nA and 10nA at 125°C, producing errors of 50 ppm and 5.4 ppm, respectively. Again the DAC is the critical error source.

To determine the significance of the error contribution of a specific Power Op Amp to the performance of various systems, refer to Table 1. The least significant bit (LSB) is the value of the smallest step change of output. Comparing the calculated errors to the LSB values reveals system compatibility. For current output DAC's, op amp bias currents compare directly with the DAC current LSB and $V_{OS}$ errors compare directly with the full scale output voltage. Thus, the importance of low bias currents is dependent solely on system resolution but the significance of voltage offset specifications varies with both resolution and full scale voltage range.

## USING VOLTAGE OUTPUT DACS

When using a voltage output DAC, the Power Op Amp can be added with either inverting or non-inverting gain to form the PPS. It usually costs more than implimentation with a current output DAC and has less accuracy. However, system or logistic factors may dictate the use of the voltage output DAC.

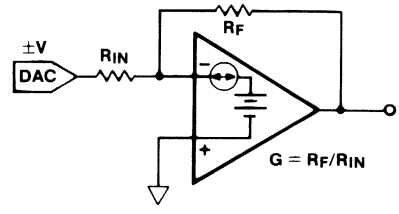



**FIGURE 2. INVERTING VOLTAGE GAIN.**

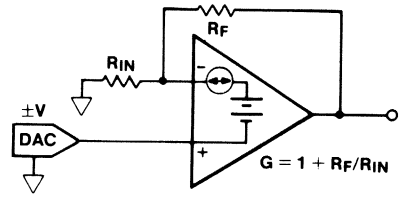



**FIGURE 3. NON-INVERTING VOLTAGE GAIN.**

Figure 2 illustrates the basic inverting gain version and Figure 3 shows a non-inverting setup. Error calculations are still simple even though some new variables have been added. Voltage offset errors appear at the output multiplied by the gain of the circuit (G+1 for inverting circuits). To maximize accuracy, the highest output DAC's should be used with minimum voltage gains in the op amp configuration. When using ±10V DAC's, a direct $V_{OS}$ to LSB comparison can be made using the 20V FSR values listed in Table 1. Also, bias currents flow through the feedback resistor producing output voltage errors. Thus values of $R_F$ and $R_{IN}$ are usually kept as low as possible.

## A CASE FOR REMOTE SENSING

The circuit of Figure 4 shows the wire resistance ($R_W$) from the Power Op Amp to the load and back to the local ground via the power return line. A 5A load current across only 0.05Ω in each line would produce a 0.5V IR drop. Without remote sensing, this would become an error at the load.

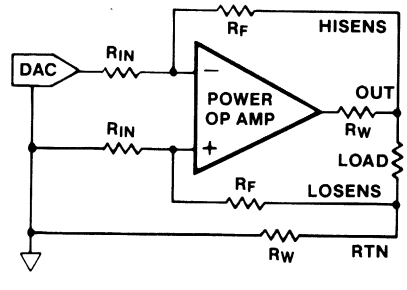



**FIGURE 4. A REMOTE SENSING PROGRAMMABLE POWER SUPPLY.**

With the addition of the second ratio matched $F_F/R_{IN}$ pair and two low current sense wires, IR drops in the power return line become common mode voltages for which the op amp has a very high rejection ratio. Voltage drops in the output and power return wires are inside the feedback loop. Therefore, as long as the Power Op Amp has the voltage drive capability to overcome the IR losses, accuracy remains high.

## CURRENT OUTPUT VERSIONS

A current output PPS using a current output DAC can be implimented as shown in Figure 5. Another version of the current output PPS is shown in Figure 6. This allows the load to be grounded, but is more complex and has additional errors. Especially if the output currents are relatively low, the current through the lower $R_F/R_{IN}$ pair may become significant because it is also sensed by $R_S$. Major errors can be caused by ratio mismatching between the $R_F/R_{IN}$ pairs. The resulting voltage errors across the sense resistor equal the output voltage times the ratio mismatch. For example, consider a 0.2Ω sense resistor, a 5A output requiring a 20V drive and a ratio mismatch of only 0.1% causes an error of 2%. Even a 8 bit LSB is only 0.39%!!

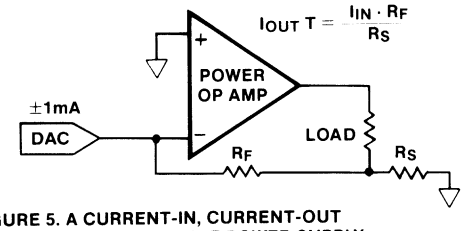



**FIGURE 5. A CURRENT-IN, CURRENT-OUT PROGRAMMABLE POWER SUPPLY.**

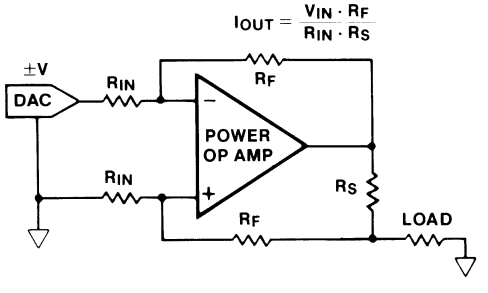



**FIGURE 6. CURRENT-OUT FOR A GROUNDED LOAD.**

In all of the current output circuits discussed, errors due to voltage offset appear across the sense resistor at a gain of one or more. This means higher sense resistor values will minimize output current errors at the expense of increased power dissipation in $R_S$, the Power Op Amp and system power supplies. One other word of caution, if the load contains inductive elements, refer to Applications Note 5 which discusses maintaining stability in precision current output circuits having reactive loads such as deflection coils.

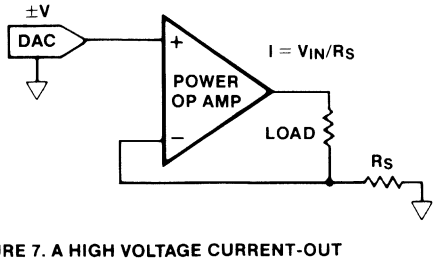



**FIGURE 7. A HIGH VOLTAGE CURRENT-OUT PROGRAMMABLE SUPPLY.**

A current output PPS using a voltage output DAC is shown in Figure 7. The Power Op Amp drives current through the load until voltage on the sense resistor ($R_S$) equals the input voltage. To achieve high efficiency (low voltage across $R_S$ compared to the load voltage), this circuit requires a low voltage DAC or a high voltage op amp. If neither is possible, the circuit of Figure 8 allows the sense resistor voltage drop to be lower than the input voltage.

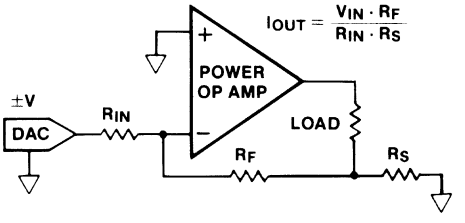



**FIGURE 8. A HIGH CURRENT, CURRENT-OUT PROGRAMMABLE POWER SUPPLY.**

## PROGRAMMABLE ACTIVE LOADS

To obtain the V-I characteristics of a power source, it may be desirable to control the output voltage and measure the output current or visa versa. The current output circuits shown are suitable as active current loads. The circuit of Figure 9 performs voltage loading of a solar cell panel. The Power Op Amp forces the DAC voltage to appear across the panel and also performs an I to V conversion providing the data to plot V-I characteristics.

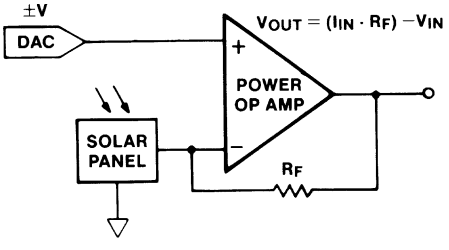


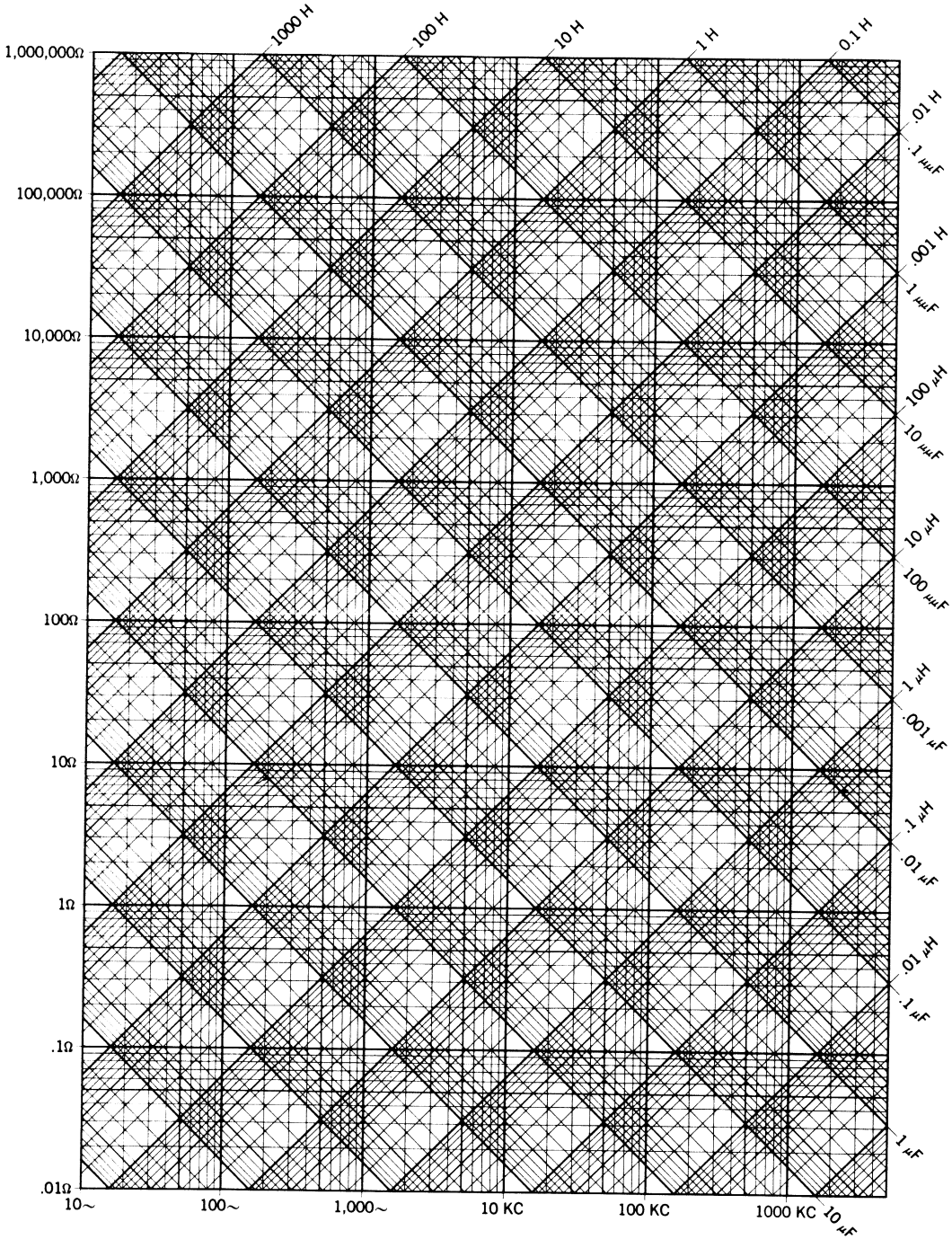

**FIGURE 9. SOLAR PANEL TESTER.**

Due to its flexibility, accuracy and ease of use, the Power Op Amp is the leading choice when Programmable Power Supplies are called for. They greatly simplify circuits requiring unipolar outputs and are very cost effective when designing bipolar power supplies. The only remaining question is whether to buy the Power Op Amp or to make one in discrete form. For low quantity production runs, the required design effort makes the "make" option too expensive. For high volume runs, the question is more involved. In many applications, the smaller size and lower weight plus high reliability, make the "buy" decision the only reasonable choice. (See the advantages of IC Power Op Amps) In all applications, the hybrid Power Op Amp enhances design quality, speeds assembly and reduces overhead costs.

| | FULL SCALE RANGE | | | | |
|---|---|---|---|---|---|
| BITS | PPM | 2mA | 20V | 50V | 200V |
| 8 | 3906 | 7.8μA | 78mV | 195mV | .78V |
| 10 | 977 | 1.95μA | 19.5mV | 48.8mV | 195mV |
| 12 | 244 | 488nA | 4.88mV | 12.2mV | 48.8mV |
| 14 | 61 | 122nA | 1.22mV | 3.05mV | 12.2mV |
| 16 | 15.3 | 30.5nA | 305μV | .763mV | 3.05mV |

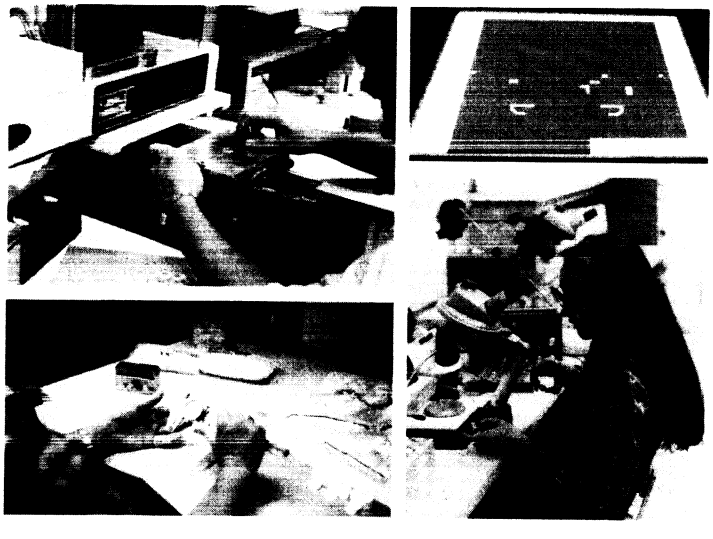
**TABLE 1. LSB VALUES FOR VARIOUS OUTPUT LEVELS.**

# REACTANCE CHART



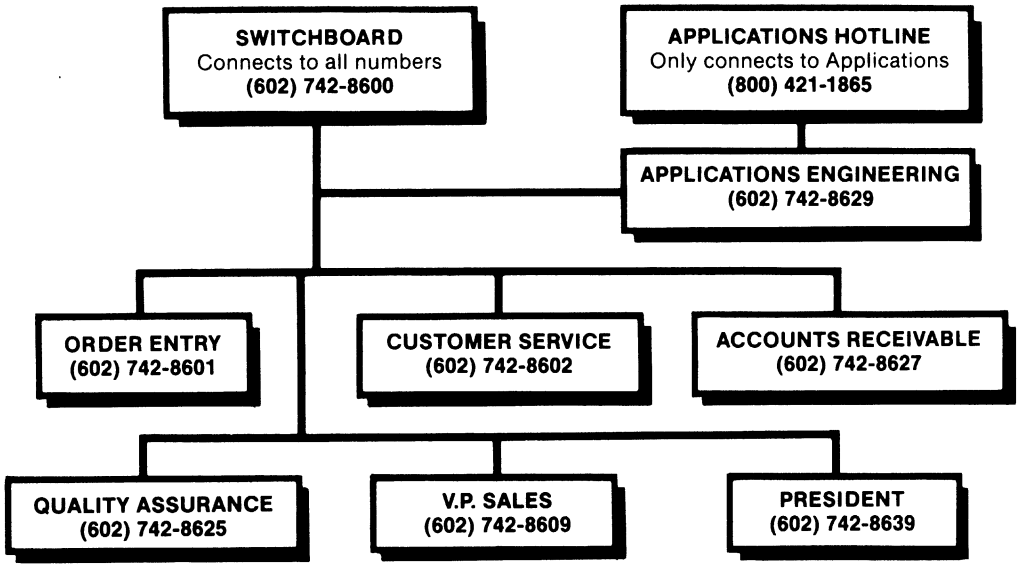
# •INDUSTRIAL MODELS

***Power for the tools that shape today's world,***
***Cost effective drives . . .***
***up to 30 Amps or***
***up to 290 V p-p . . .***



# ACCESS DIRECTORY

## TELEX: 170631




## STANDARD HOURS:

| | MOUNTAIN STANDARD TIME | GREENWICH MEAN TIME |
|---|---|---|
| SWITCH BOARD: | 8:00 AM to 4:30 PM | 15:00 to 23:30 |
| ORDER ENTRY: | 7:00 AM to 5:00 PM | 14:00 to 24:00 |
| OTHER: | 8:00 AM to 4:00 PM | 15:00 to 23:00 |

**APEX MICROTECHNOLOGY CORP. (Domestic)**
**APEX F.S.C. INC. (Export)**
5980 N. SHANNON ROAD, TUCSON, AZ 85741, USA

# PA01 • PA11 • PA73

## POWER OPERATIONAL AMPLIFIERS

## FEATURES

- LOW COST, ECONOMY MODEL — PA01
- SECOND SOURCEABLE — PA11 & PA73
- HIGH OUTPUT CURRENT — Up to ±5A PEAK
- EXCELLENT LINEARITY — PA01 & PA11
- HIGH SUPPLY VOLTAGE — Up to ±34V
- ISOLATED CASE — 300V

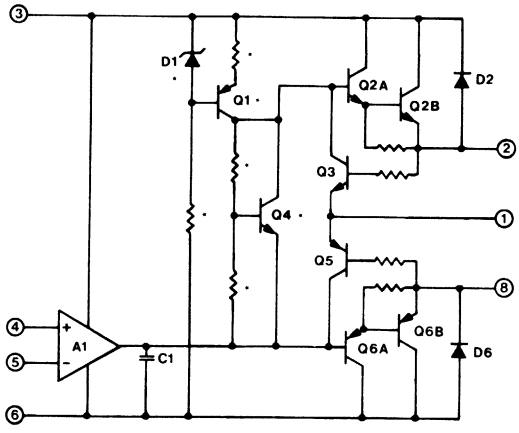
## APPLICATIONS

- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 20KHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 56V
- AUDIO AMPLIFIERS UP TO 50W RMS

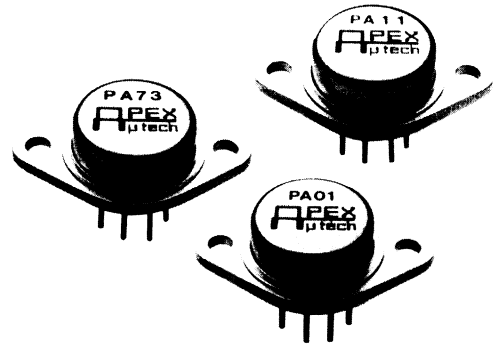
## DESCRIPTION

The PA01, PA11 and PA73 are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. All three have a complimentary darlington emitter follower output stage protected against inductive kick-back or back EMF. For optimum linearity, the PA01 and PA11 have a class A/B output stage. The PA73 has a simple class C output stage (see Note 1) to reduce cost for motor control and other applications where crossover distortion is not critical and to provide interchangeability with type 3573 amplifiers. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limit resistors. These amplifiers are internally compensated for all gain settings. For continuous operation under load, a heat sink of proper rating is recommended.

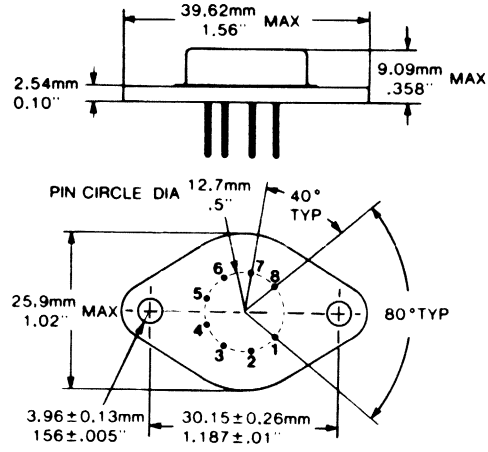
These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is hermetically sealed by resistance welding.




NOTE 1 *Indicates not used in PA73. Open base of Q2A connected to output of A1.

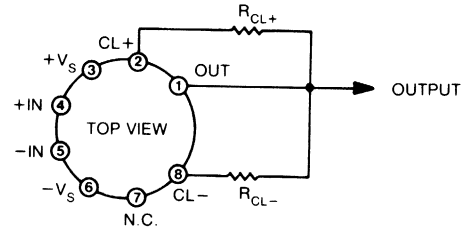



## PACKAGE OUTLINE




| | |
|---|---|
| PIN DIAMETER: | 1.01mm or 0.04" |
| PIN LENGTH: | 10.2mm or 0.40" MIN |
| PIN MATERIAL: | Nickel plated alloy 52, solderable |
| PACKAGE: | Hermetic, nickel plated steel |
| ISOLATION: | 300VDC any pin to case |
| SOCKETS: | APEX PN: MS03 |
| CAGE JACKS: | APEX PN: MS02 (set of 8) |
| HEATSINKS: | APEX PNs: HS01 thru HS05 |

## EXTERNAL CONNECTIONS



# PA01, 11, 73 ABSOLUTE MAXIMUM RATINGS

| | PA01 | PA11, PA73 |
|---|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 60V | 68V |
| OUTPUT CURRENT, source | 5A | 5A |
| OUTPUT CURRENT, sink | see SOA | see SOA |
| POWER DISSIPATION, internal[1] | 67W | 67W |
| INPUT VOLTAGE, differential | $\pm V_S$ −3V | $\pm V_S$ −3V |
| INPUT VOLTAGE, common-mode | $\pm V_S$ | $\pm V_S$ |
| TEMPERATURE, junction[1] | 200°C | 200°C |
| TEMPERATURE, pin solder-10s | 300°C | 300°C |
| TEMPERATURE RANGE, storage | −65 to +150°C | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −25 to +85°C | −25 to +85°C |

# SPECIFICATIONS

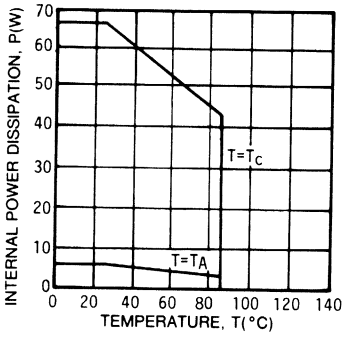
| | | PA01 | | | PA11/PA73 | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[2]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C$ = 25°C | | ±5 | ±12 | | * | ±10 | mV |
| OFFSET VOLTAGE, vs. temperature | Full temperature range | | ±10 | ±65 | | * | * | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C$ = 25°C | | ±35 | | | * | ±200 | µV/V |
| OFFSET VOLTAGE, vs. power | $T_C$ = 25°C | | ±20 | | | * | | µV/W |
| BIAS CURRENT, initial | $T_C$ = 25°C | | ±15 | ±50 | | * | ±40 | nA |
| BIAS CURRENT, vs. temperature | Full temperature range | | ±.05 | ±.4 | | * | * | nA/°C |
| BIAS CURRENT, vs. supply | $T_C$ = 25°C | | ±.02 | | | * | | nA/V |
| OFFSET CURRENT, initial | $T_C$ = 25°C | | ±5 | ±15 | | * | ±10 | nA |
| OFFSET CURRENT, vs. temperature | Full temperature range | | ±.01 | | | * | | nA/°C |
| INPUT IMPEDANCE, common-mode | $T_C$ = 25°C | | 200 | | | * | | MΩ |
| INPUT IMPEDANCE, differential | $T_C$ = 25°C | | 10 | | | * | | MΩ |
| INPUT CAPACITANCE | $T_C$ = 25°C | | 3 | | | * | | pF |
| COMMON-MODE VOLTAGE RANGE[3] | Full temperature range | $\pm V_S$ −6 | $\pm V_S$ −3 | | * | * | | V |
| COMMON-MODE REJECTION, dc[3] | $T_C$ = 25°C, $V_{CM}$ = $V_S$ −6V | 70 | 110 | | * | * | | db |
| **GAIN** | | | | | | | | |
| OPEN LOOP GAIN at 10Hz | Full temp. range, full load | 91 | 113 | | * | * | | db |
| GAIN BANDWIDTH PRODUCT at 1MHz | $T_C$ = 25°C, full load | | 1 | | | * | | MHz |
| POWER BANDWIDTH | $T_C$ = 25°C, $I_O$ = 4A, $V_O$ = 40$V_{PP}$ | 15 | 23 | | * | * | | kHz |
| PHASE MARGIN | Full temperature range | | 45 | | | * | | ° |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[3] | $T_C$ = 25°C, $I_O$ = 5A | $\pm V_S$ −10 | $\pm V_S$ −5 | | $\pm V_S$ −8 | * | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 2A | $\pm V_S$ −6 | $\pm V_S$ −5 | | * | * | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 46mA | $\pm V_S$ −5 | | | * | | | V |
| CURRENT, peak | $T_C$ = 25°C | ±5 | | | * | | | A |
| SETTLING TIME to .1% | $T_C$ = 25°C, 2V step | | 2 | | | * | | µs |
| SLEW RATE | $T_C$ = 25°C, $R_L$ = 2.5Ω | ±1.0 | 2.6 | | * | * | | V/µs |
| CAPACITIVE LOAD, unity gain | Full temperature range | | | 3.3 | | | * | nF |
| CAPACITIVE LOAD, gain>4 | Full temperature range | | | SOA | | | * | |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | Full temperature range | ±10 | ±28 | ±28 | * | * | ±30 | V |
| CURRENT, quiescent | $T_C$ = 25°C | | 20 | 50 | | 20/2.6 | 30/5 | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac[4] junction to case | F>60Hz | | 1.9 | 2.1 | | * | * | °C/W |
| RESISTANCE, dc junction to case | F<60Hz | | 2.4 | 2.6 | | * | * | °C/W |
| RESISTANCE, junction to air | | | 30 | | | * | | °C/W |
| TEMPERATURE RANGE, case | Meet full range specification | −25 | 25 | +85 | * | * | * | °C |

**NOTES:** * The specification of PA11/PA73 is identical to the specification for PA01 in applicable column to the left.

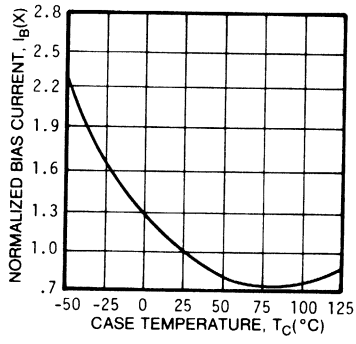
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total $V_S$ is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
6. The PA73M is screened to MIL-STD-883C Class B Method 5008. See military models.

# PA01, 11, 73 TYPICAL PERFORMANCE GRAPHS

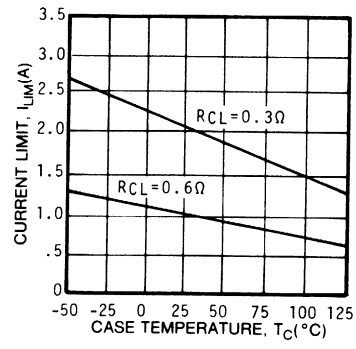
### POWER DERATING



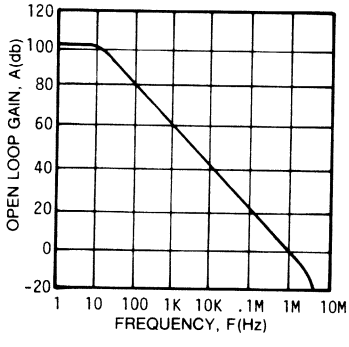

### BIAS CURRENT



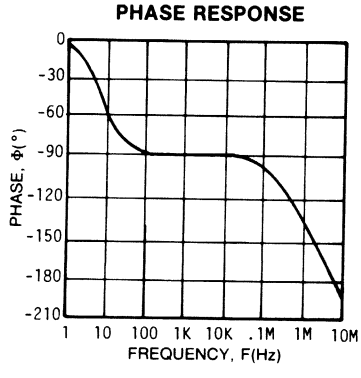

### CURRENT LIMIT



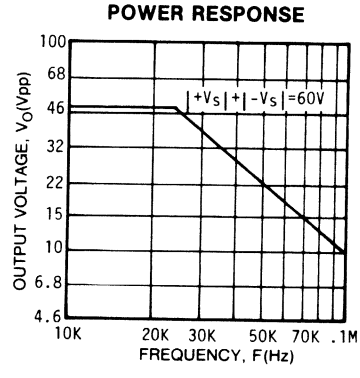

### SMALL SIGNAL RESPONSE



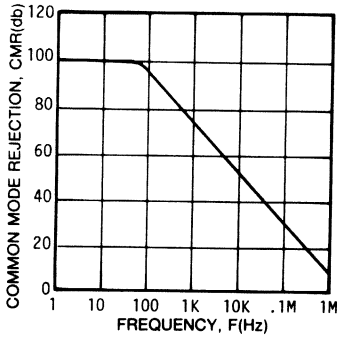

### PHASE RESPONSE



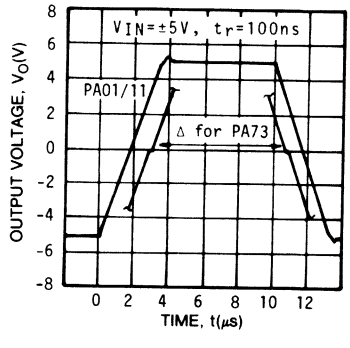

### POWER RESPONSE



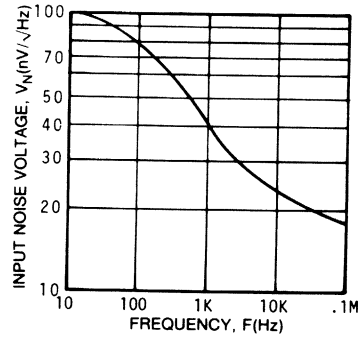

### COMMON MODE REJECTION



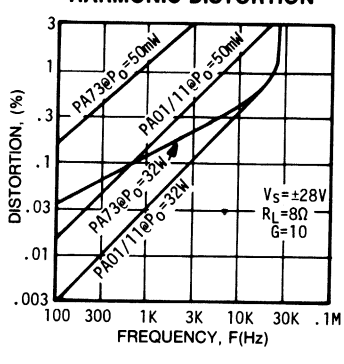

### PULSE RESPONSE



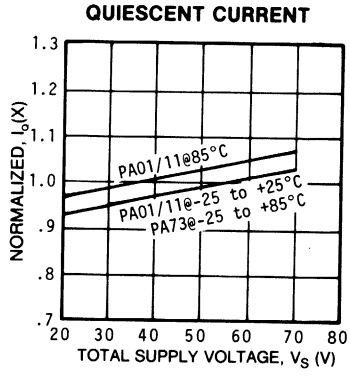

### INPUT NOISE



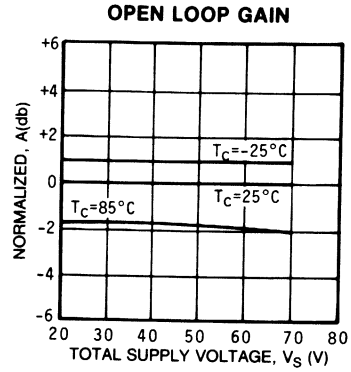

### HARMONIC DISTORTION




### QUIESCENT CURRENT




### OPEN LOOP GAIN

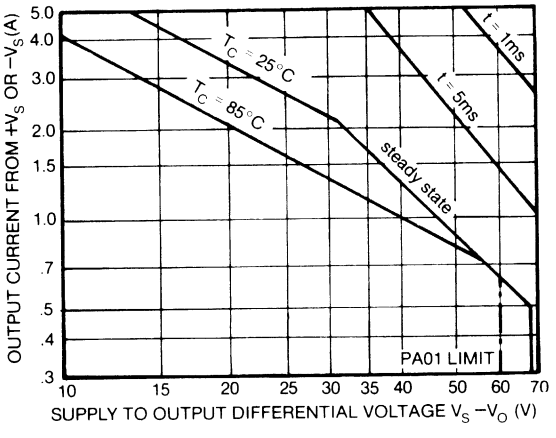


## GENERAL

Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks and mating sockets, see the "Package Outline" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

## SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:
1. The current handling capability of the transistor geometry and the wire bonds.
2. The secondary breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.




The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. Capacitive and dynamic* inductive loads up to the following maximums are safe with the current limits set as specified:

| | CAPACITIVE LOAD | | INDUCTIVE LOAD | |
|---|---|---|---|---|
| $\pm V_S$ | $I_{LIM}$ = 2A | $I_{LIM}$ = 5A | $I_{LIM}$ = 2A | $I_{LIM}$ = 5A |
| 30V | 1,200μF | 500μF | 250mH | 24mH |
| 25V | 4,000μF | 1,600μF | 400mH | 38mH |
| 20V | 20,000μF | 5,000μF | 1,500mH | 75mH |
| 15V | ** | 25,000μF | ** | 100mH |

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with $I_{LIM}$ = 5A or 20V below the supply rail with $I_{LIM}$ = 2A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.
**Secondary breakdown effect imposes no limitation but thermal limitations must still be observed.

2. EMF generating or reactive load and short circuits to the supply rails or shorts to common are safe if the current limits are set as follows at $T_C$ = 85°C:

| $\pm V_S$ | SHORT TO $\pm V_S$, C, L or EMF LOAD | SHORT TO COMMON |
|---|---|---|
| 34V | .50A | 1.2A |
| 30V | .60A | 1.3A |
| 25V | .75A | 1.6A |
| 20V | 1.0A | 2.1A |
| 15V | 1.3A | 2.8A |

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

# PA02 • PA02A

## POWER OPERATIONAL AMPLIFIERS

## FEATURES

- HIGH POWER BANDWIDTH — 350KHz
- HIGH SLEW RATE — 20V/μs
- FAST SETTLING TIME — 600 ns
- LOW CROSSOVER DISTORTION — Class A/B
- LOW INTERNAL LOSSES — 1.2V at 2A
- HIGH OUTPUT CURRENT — ±5A Peak
- LOW INPUT BIAS CURRENT — FET Input
- ISOLATED CASE — 300 VDC

## APPLICATIONS

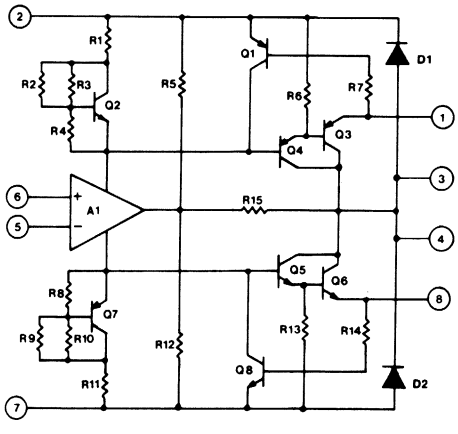
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 5A
- POWER TRANSDUCERS UP TO 350 KHz
- AUDIO AMPLIFIERS UP TO 30W RMS

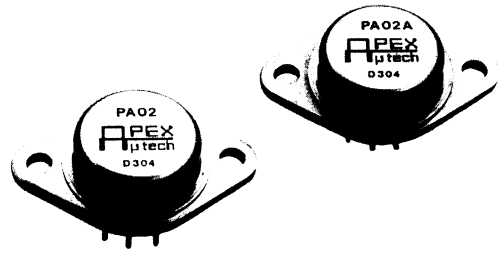
## DESCRIPTION

The PA02 and PA02A are wideband, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complimentary common collector output stage can swing close to the supply rails and is protected against inductive kickback. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors (down to 10mA). Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heat sink of proper rating is recommended. Do not use isolation washers!

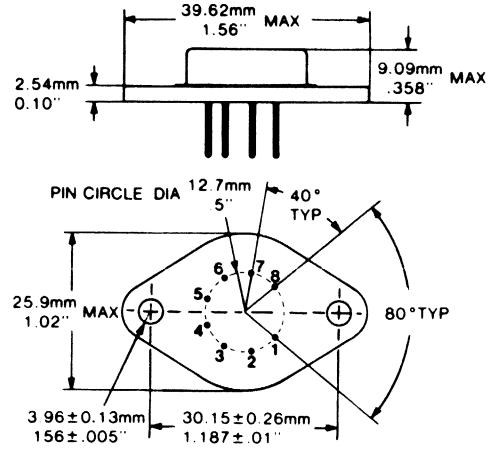
These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is isolated and hermetically sealed.

## SCHEMATIC



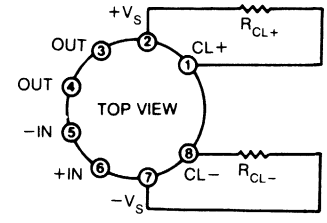




## PACKAGE OUTLINE




| | |
|---|---|
| PIN DIAMETER: | 1.01mm or 0.04" |
| PIN LENGTH: | 10.2mm or 0.40" MIN |
| PIN MATERIAL, STD: | Nickel plated alloy 52, solderable |
| PIN MATERIAL, MIL: | Gold or nickel plated alloy 52, solderable |
| PACKAGE: | Hermetic, nickel plated steel |
| ISOLATION: | 300VDC any pin to case |
| SOCKETS: | APEX PN: MS03 |
| CAGE JACKS: | APEX PN: MS02 (set of 8) |
| HEATSINKS: | APEX PNs: HS01 thru HS05 |

## EXTERNAL CONNECTIONS



# PA02 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 38V |
| OUTPUT CURRENT, source | 5A |
| OUTPUT CURRENT, sink | see SOA |
| POWER DISSIPATION, internal[1] | 48W |
| INPUT VOLTAGE, differential | $\pm V_S$ −5V |
| INPUT VOLTAGE, common-mode | $\pm V_S$ −2V |
| TEMPERATURE, pin solder-10s | 300°C |
| TEMPERATURE, junction[1] | 150°C |
| TEMPERATURE RANGE, storage | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −55 to +125°C |

# SPECIFICATIONS

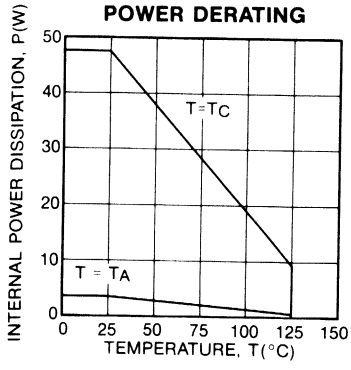
| | | PA02 | | | PA02A | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[2]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C$ = 25°C | | ±5 | ±10 | | ±1 | ±3 | mV |
| OFFSET VOLTAGE, vs. temperature | Full temperature range | | ±10 | ±50 | | * | ±25 | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C$ = 25°C | | ±10 | | | * | | µV/V |
| OFFSET VOLTAGE, vs. power | $T_C$ = 25°C | | ±6 | | | * | | µV/W |
| BIAS CURRENT, initial | $T_C$ = 25°C | | 50 | 200 | | 25 | 100 | pA |
| BIAS CURRENT, vs. temperature | $T_C$ = 85°C | | | 60 | | | * | nA/°C |
| BIAS CURRENT, vs. supply | $T_C$ = 25°C | | .01 | | | * | | pA/V |
| OFFSET CURRENT, initial | $T_C$ = 25°C | | 25 | 100 | | 15 | 50 | pA |
| OFFSET CURRENT, vs. temperature | $T_C$ = 85°C | | | 15 | | | * | nA/°C |
| INPUT IMPEDANCE, dc | $T_C$ = 25°C | | 1000 | | | * | | GΩ |
| INPUT CAPACITANCE | $T_C$ = 25°C | | 3 | | | * | | pF |
| COMMON-MODE VOLT. RANGE,[3] Pos. | Full temperature range | $\pm V_S$ −6 | $\pm V_S$ −3 | | * | * | | V |
| COMMON-MODE VOLT. RANGE,[3] Neg. | Full temperature range | $\pm V_S$ +6 | $\pm V_S$ +5 | | * | * | | V |
| COMMON-MODE REJECTION, dc | Full temperature range | 70 | 100 | | | * | | db |
| **GAIN** | | | | | | | | |
| OPEN LOOP GAIN at 10Hz | $T_C$ = 25°C, 1kΩ load | | 103 | | | * | | db |
| OPEN LOOP GAIN at 10Hz | Full temp, range, 10Ω load | 86 | 100 | | * | * | | db |
| GAIN BANDWIDTH PRODUCT at 1MHz | $T_C$ = 25°C, 10Ω load | | 4.5 | | | * | | MHz |
| POWER BANDWIDTH | $T_C$ = 25°C, 10Ω load | | 350 | | | * | | kHz |
| PHASE MARGIN | Full temp. range, 10Ω load | | 45 | | | * | | ° |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[3] | $T_C$ = 25°C, $I_O$ = 5A, $R_{CL}$ = .08Ω | $\pm V_S$ −4 | $\pm V_S$ −3 | | * | * | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 2A | $\pm V_S$ −2 | $\pm V_S$−1.2 | | * | * | | V |
| CURRENT, peak | $T_C$ = 25°C | 5 | | | * | | | A |
| SETTLING TIME to .1% | $T_C$ = 25°C, 2V step | | .6 | | | * | | µs |
| SLEW RATE | $T_C$ = 25°C | 13 | 20 | | * | * | | V/µs |
| CAPACITIVE LOAD | Full temp. range, G >10 | | SOA | | | * | | |
| HARMONIC DISTORTION | $P_O$ = .5W, F = 1kHz, $R_L$ = 10Ω | | .004 | | | * | | % |
| SMALL SIGNAL rise/fall time | $R_L$ = 10Ω, G = 1 | | 100 | | | * | | ns |
| SMALL SIGNAL overshoot | $R_L$ = 10Ω, G = 1 | | 10 | | | * | | % |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | Full temperature range | ±7 | ±15 | ±19 | * | * | * | V |
| CURRENT, quiescent | $T_C$ = 25°C | | 27 | 37 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac[4] junction to case | F>60Hz | | 1.9 | 2.1 | | * | * | °C/W |
| RESISTANCE, dc junction to case | F<60Hz | | 2.4 | 2.6 | | * | * | °C/W |
| RESISTANCE, junction to air | | | 30 | | | * | | °C/W |
| TEMPERATURE RANGE, case | Meet full range specification | −25 | | +85 | −55 | | +125 | °C |

**NOTES:** * The specification of PA02A is identical to the specification for PA02 in applicable column to the left.

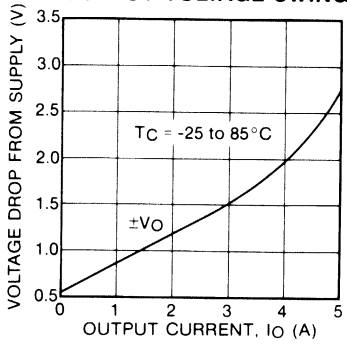
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total $V_S$ is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850° C to avoid generating toxic fumes.
6. The PA02M is screened to MIL-STD-883C Class B Method 5008. See military models.

# PA02 TYPICAL PERFORMANCE GRAPHS

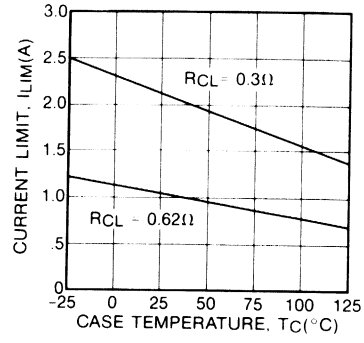
### POWER DERATING



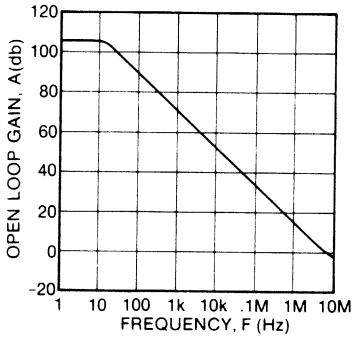

### OUTPUT VOLTAGE SWING



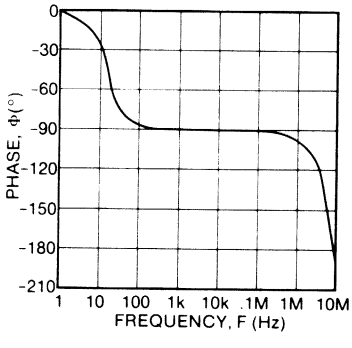

### CURRENT LIMIT



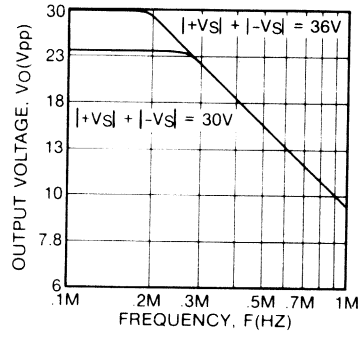

### SMALL SIGNAL RESPONSE



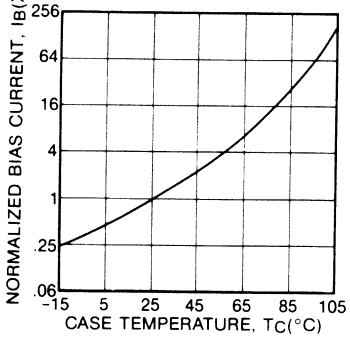

### PHASE RESPONSE



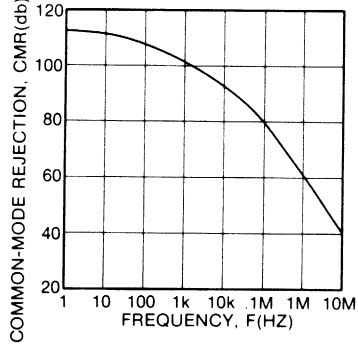

### POWER RESPONSE



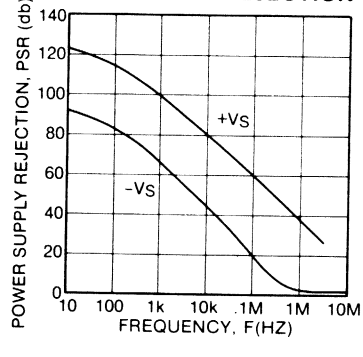

### BIAS CURRENT



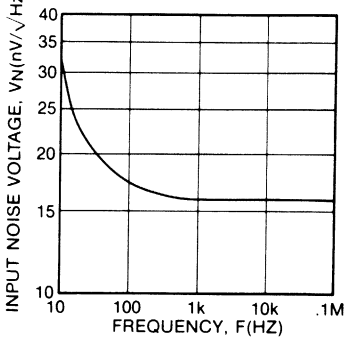

### COMMON-MODE REJECTION



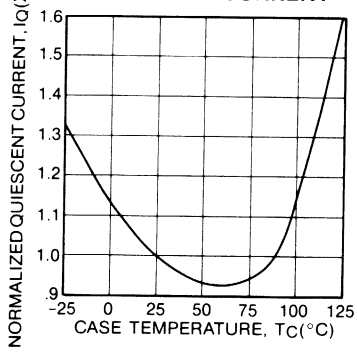

### POWER SUPPLY REJECTION



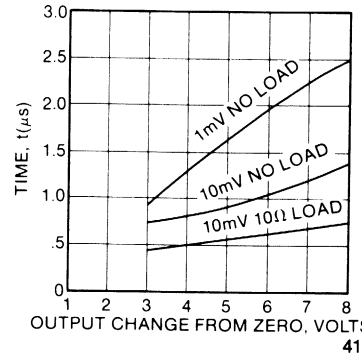

### INPUT NOISE



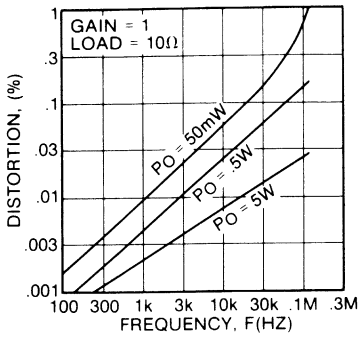

### QUIESCENT CURRENT



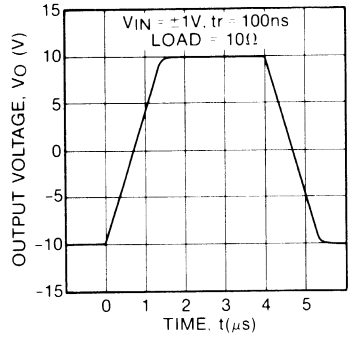

### SETTLING TIME



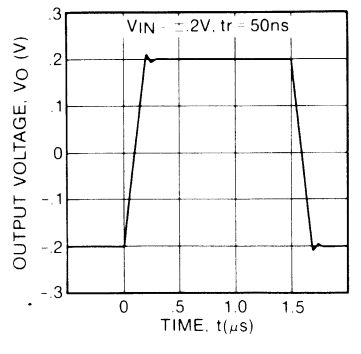
## HARMONIC DISTORTION



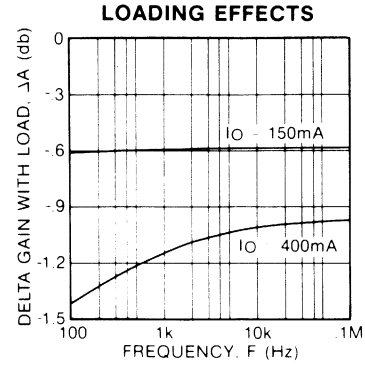

## PULSE RESPONSE




## PULSE RESPONSE




## LOADING EFFECTS

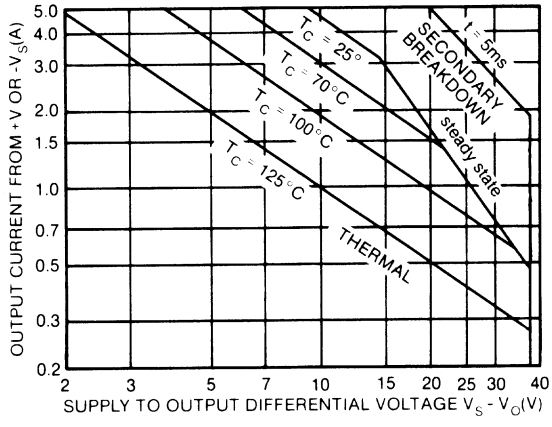



# PA02 OPERATING CONSIDERATIONS

## GENERAL

Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks and mating sockets, see the "Package Outline" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

## SAFE OPERATING AREA (SOA)




The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximums are safe:

| | CAPACITIVE LOAD | | INDUCTIVE LOAD | |
|---|---|---|---|---|
| $\pm V_S$ | $I_{LIM}$ = 2A | $I_{LIM}$ = 5A | $I_{LIM}$ = 2A | $I_{LIM}$ = 5A |
| 18V | 2mF | 0.7mF | .2H | 10mH |
| 15V | 10mF | 2.2mF | .7H | 25mH |
| 10V | 25mF | 10mF | 5H | 50mH |

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with $I_{LIM}$ = 5A or 17V below the supply rail with $I_{LIM}$ = 2A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or shorts to common if the current limits are set as follows at $T_C$ = 85 C:

| $\pm V_S$ | SHORT TO $\pm V_S$, C, L OR EMF LOAD | SHORT TO COMMON |
|---|---|---|
| 18V | .5A | 1.7A |
| 15V | .7A | 2.8A |
| 10V | 1.6A | 4.2A |

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

## DEVICE MOUNTING

The case (mounting flange) is electrically-isolated and should be mounted directly to a heat sink with thermal compound but without using an insulating washer or spacer. Screws with Bellville spring washers are recommended to maintain positive clamping pressure on heat sink mounting surfaces. Long periods of thermal cycling can loosen mounting screws and increase thermal resistance.

## CASE GROUNDING

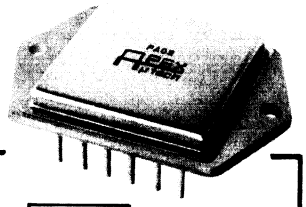
Since the case is electrically isolated (floating) with respect to the internal circuits it is recommended to connect it, or the heat sink it is mounted on to common or other convenient AC ground potential.

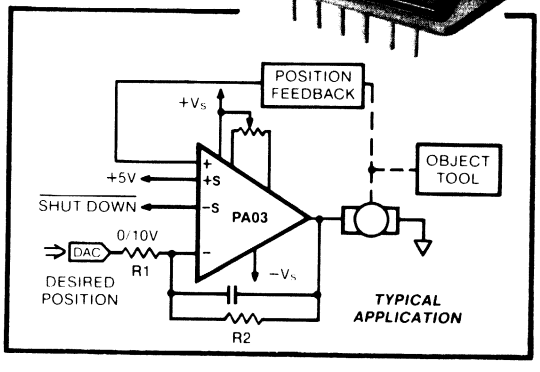
# PA03 • PA03A

## POWER OPERATIONAL AMPLIFIER

## FEATURES

- **POWER DIP™ PACKAGE - 500 Watts**
- **HIGH VOLTAGE OPERATION - ±75V**
- **VERY HIGH CURRENT - ±30 Amps**
- **INTERNAL SOA PROTECTION**
- **OUTPUT SWINGS CLOSE TO SUPPLY RAILS**
- **EXTERNAL SHUT DOWN CONTROL**






## APPLICATIONS

- **LINEAR AND ROTARY MOTOR DRIVES**
- **YOKE/MAGNETIC FIELD EXITATION**
- **PROGRAMMABLE POWER SUPPLIES TO ±72V**
- **TRANSDUCER/AUDIO UP TO 1000W**

## DESCRIPTION

The super power PA03 advances the state of the art in both brute force power and self protection against abnormal operating conditions. Its features start with a copper dip package developed by APEX to extend power capabilities well beyond those attainable with the familiar TO-3 package. The increased pin count of the new package provides additional control features, while the superior thermal conductivity of copper allows substantially higher power ratings.

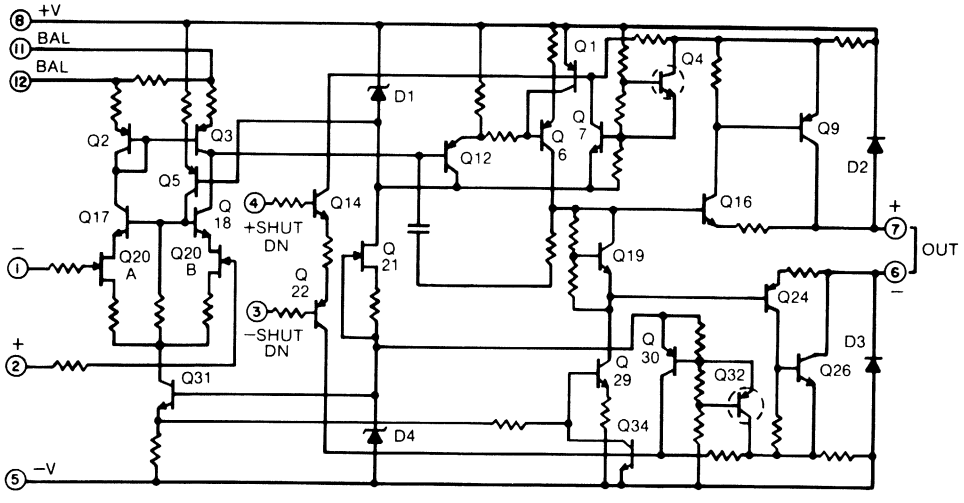
The PA03 incorporates innovative current limiting circuits limiting internal power dissipation to a curve approximating the safe operating area of the power transistors. The internal current limit of 35A is supplemental with thermal sensing which reduces the current limit as the substrate temperature rises. Furthermore, a subcircuit monitors actual junction temperatures and with a response time of less than one millisecond reduces the current limit further to keep the junction temperature at 175°C. This new approach makes the device nearly indestructible.

The PA03 also features a laser trimmed high performance FET input stage providing superior DC accuracies both initially and over the full temperature range.

These hybrid integrated circuits utilize thick film conductors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 12 pin Power Dip (TM) package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. Insulating washers are not recommended.

**IMPORTANT: OBSERVE MOUNTING PRECAUTIONS.**

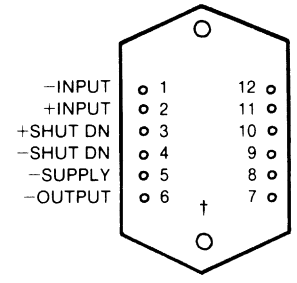
## EQUIVALENT SCHEMATIC



# PA03 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 150V |
| OUTPUT CURRENT, source | Internally Limited |
| POWER DISSIPATION, internal | 500W |
| INPUT VOLTAGE, differential | ±50V |
| INPUT VOLTAGE, common-mode | $\pm V_S$ |
| TEMPERATURE, pin solder-10s | 300°C |
| TEMPERATURE, junction[1] | 175°C |
| TEMPERATURE RANGE, storage | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −55 to +125°C |
| SHUT DOWN VOLTAGE, differential | ±5V |
| SHUT DOWN VOLTAGE, common mode | $\pm V_S$ |

# EXTERNAL CONNECTIONS




Pins 6 & 7 must be connected together

†**IMPORTANT: OBSERVE MOUNTING PRECAUTIONS.**

# SPECIFICATIONS

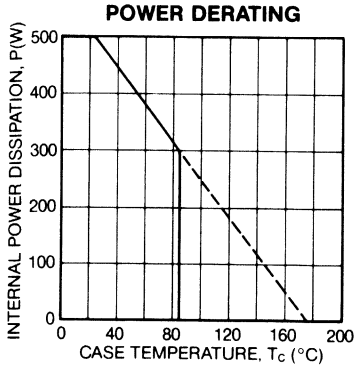
| | | PA03 | | | PA03A | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[2]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C$ = 25°C | | ±.5 | ±2 | | ±.25 | ±.5 | mV |
| OFFSET VOLTAGE, vs. temperature | Full temperature range | | 10 | 30 | | 5 | 10 | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C$ = 25°C | | 8 | | | * | | µV/V |
| OFFSET VOLTAGE, vs. power | Full temperature range | | 20 | | | 10 | | µV/W |
| BIAS CURRENT, initial | $T_C$ = 25°C | | 5 | 50 | | 3 | 10 | pA |
| BIAS CURRENT, vs. supply | $T_C$ = 25°C | | .01 | | | * | | pA/V |
| OFFSET CURRENT, initial | $T_C$ = 25°C | | 2.5 | 50 | | 1.5 | 10 | pA |
| INPUT IMPEDANCE, dc | $T_C$ = 25°C | | $10^{11}$ | | | * | | Ω |
| INPUT CAPACITANCE | $T_C$ = 25°C | | 6 | | | * | | pF |
| COMMON-MODE VOLTAGE RANGE[3] | Full temperature range | $\pm V_S$−10V | | | * | | | V |
| COMMON-MODE REJECTION, dc | Full temp. range, $V_{CM}$ = ±20V | 86 | 108 | | * | * | | db |
| SHUT DOWN CURRENT[4] | Full temp. range | | 100 | | | * | | µA |
| SHUT DOWN VOLTAGE | Full temp. range, operating | | | .85 | | | * | V |
| SHUT DOWN VOLTAGE | Full temp. range, disabled | 3.5 | | | * | * | | V |
| **GAIN** | | | | | | | | |
| OPEN LOOP GAIN at 10Hz | Full temp. range, full load | 92 | 102 | | | * | * | db |
| GAIN BANDWIDTH PRODUCT at 1MHz | $T_C$ = 25°C, full load | | 1 | | | * | | MHz |
| POWER BANDWIDTH | $T_C$ = 25°C, $I_O$ = 15A, $V_O$ = 88$V_{PP}$ | | 30 | | | * | | kHz |
| PHASE MARGIN | Full temp. range, $C_C$ = 1.8nF | | 65 | | | * | | ° |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[3] | $T_C$ = 25°C, $I_O$ = 30A | $\pm V_S$−7 | 6.2 | | * | * | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 12A | $\pm V_S$−5 | 4.2 | | * | * | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 146mA | $\pm V_S$−4 | 3.5 | | * | * | | V |
| CURRENT, peak | $T_C$ = 25°C | 30 | | | * | | | A |
| SETTLING TIME to .1% | $T_C$ = 25°C, 10V step | | 8 | | | * | | µs |
| SLEW RATE | $T_C$ = 25°C, $C_C$ − open | | 8 | | | * | | V/µs |
| CAPACITIVE LOAD | Full temp. range, G = 1 | 2 | | | * | | | nF |
| SHUT DOWN DELAY | $T_C$ − 25°C, disable | | 10 | | | * | | µs |
| | $T_C$ − 25°C, operate | | 20 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | Full temperature range | ±15 | ±50 | ±75 | * | * | * | V |
| CURRENT, quiescent | $T_C$ = 25°C | | 125 | 300 | | * | * | mA |
| CURRENT, disable mode | Full temperature range | | 25 | 40 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac[5] junction to case | Full temp. range, F>60Hz | | .22 | .28 | | * | * | °C/W |
| RESISTANCE, dc junction to case | Full temp. range, F<60Hz | | .25 | .3 | | * | * | °C/W |
| RESISTANCE, junction to case | Full temperature range | | 14 | | | * | | °C/W |
| TEMPERATURE, junction | Sustained operation | | | 150 | | | * | °C/W |
| TEMPERATURE RANGE, case | Meet full range specification | −25 | | 85 | * | | * | °C/W |

**NOTES:** * The specification of PA03A is identical to the specification for PA03 in applicable column to the left.

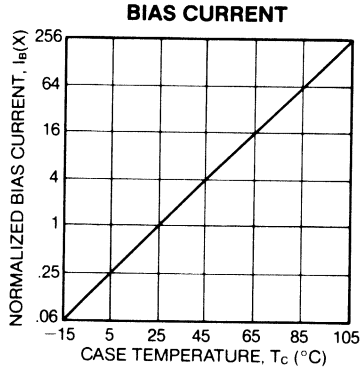
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total $V_S$ is measured from $+V_S$ to $-V_S$.
4. Rating applies if both shut down inputs are least 1V inside supply rails. If one of the shut down inputs is tied to a supply rail, the current in that pin may increase to 2.4mA.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
7. The PA03 must be used with a heatsink or the quiescent power may drive the unit into thermal shutdown.

# PA03 TYPICAL PERFORMANCE GRAPHS

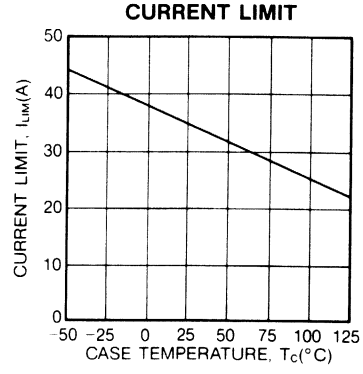
### POWER DERATING



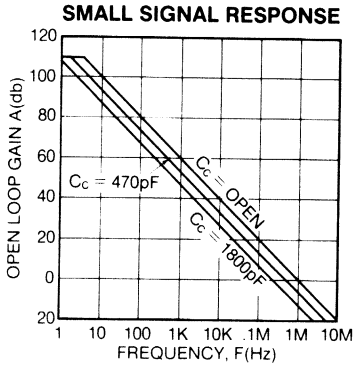

### BIAS CURRENT



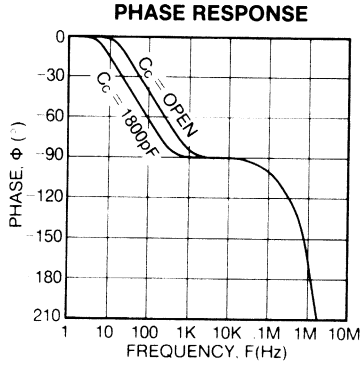

### CURRENT LIMIT



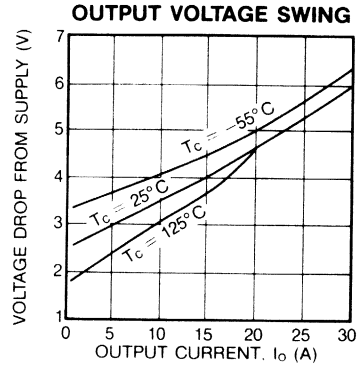

### SMALL SIGNAL RESPONSE



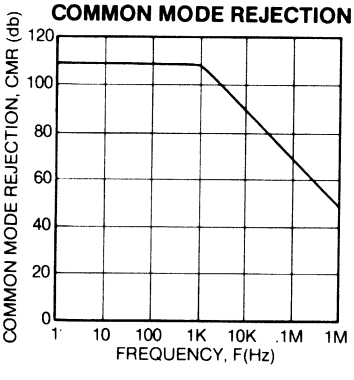

### PHASE RESPONSE



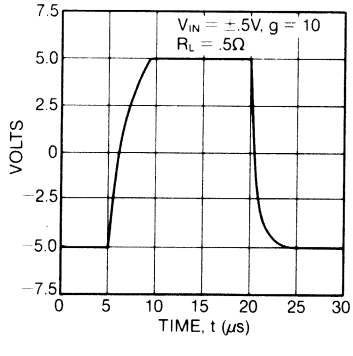

### OUTPUT VOLTAGE SWING



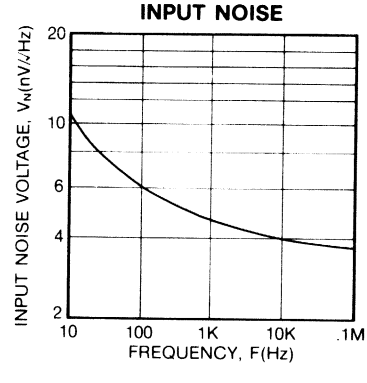

### COMMON MODE REJECTION



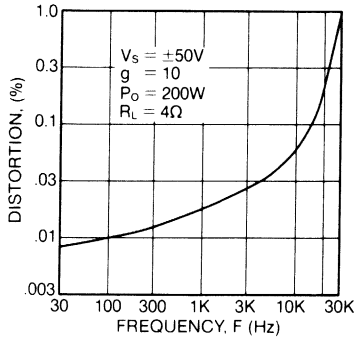

### PULSE RESPONSE



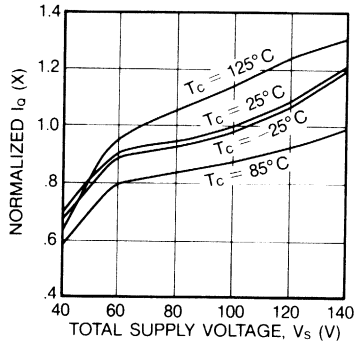

### INPUT NOISE



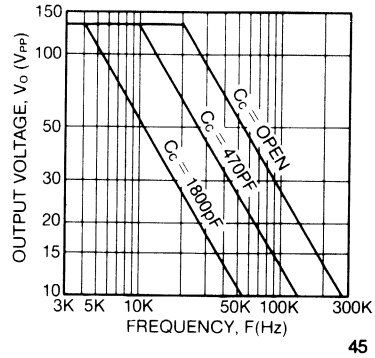

### HARMONIC DISTORTION




### QUIESCENT CURRENT




### POWER RESPONSE



# PA03 OPERATING CONSIDERATIONS

## GENERAL

Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks, and mating sockets, see the "Package Outlines" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

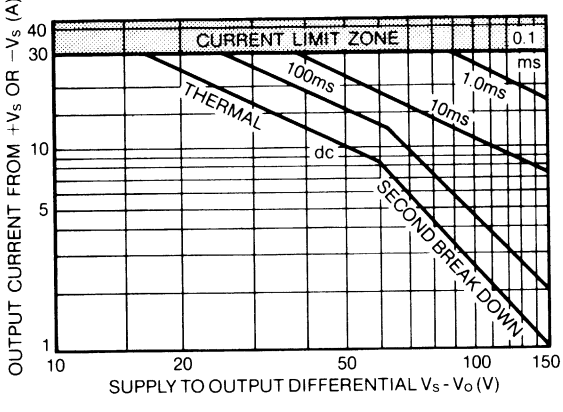
## MOUNTING PRECAUTIONS

The PA03 copper base is very soft and easily bent. Do not put any stress on the mounting ears of this package. This calls for caution when pushing the amplifier into certain types of packaging foam and particularly when inserting the device into a socket. Insert the amplifier into the socket only by pushing on the perimeter of the package lid. Pushing the unit into the socket by applying pressure to the mounting tabs will bend the base due to the high insertion force required. The base will then not contact the heatsink evenly resulting in very poor heat transfer. To remove a unit from a socket, pry the socket away from the heatsink so that the heatsink will support the amplifier base evenly.

## SAFE OPERATING AREA (SOA)

Due to the unique protection circuits of the PA03, the safe operating area (SOA) curve must be interpreted differently from the SOA of the other power op amps. The thermal shutdown circuit of the PA03 complies with the thermal limitations of the curve. This positively prevents failures.

## SAFE OPERATING AREA CURVES




Second breakdown limitations do apply to the PA03 but are less severe, since the junction temperature limiting responds within 1mS. Stress levels shown as being safe for more than 1mS duration will merely cause thermal shutdown.

While the safety features of the PA03 increase reliability, temperatures of 175°C are reached when the protection circuits activate. A design which depends on the shutdown features repetitively rather than to protect against abnormal conditions, is operating the junctions at elevated temperatures and will reduce reliability.

## BALANCE CONTROL

The voltage offset of the PA03 may be externally adjusted to zero. To implement this adjustment install a 100 to 200 ohm potentiometer between pins 11 and 12 and connect the wiper arm to the positive supply.

If the optional adjust provision is not used, connect both pins 11 and 12 to the positive supply.

## OUTPUT STAGE SHUTDOWN

The entire power stage of the PA03 may be disabled using one of the circuits shown in Figure 1. There are many applications for this function. One is a load protection based on power delivered to the load or thermal rise. Another one is conservation of power when using batteries. The control voltage requirements accommodate a wide variety logic drivers.

1. CMOS operating at +5V can drive the control pins directly.
2. CMOS operating at greater than 5V supplies need a voltage divider.
3. TTL logic needs a pull up resistor to +5V to provide a swing to the fully disabled voltage. (3.5V)

When not using the shutdown feature, connect both pins 3 and 4 to common.

## PHASE COMPENSATION

At low gain settings an external compensation capacitor is required to insure stability. In addition to the resistive feedback network, roll off or integrating capacitors must also be considered. A frequency of 1MHz is most appropriate to calculate gain. Operation at gains below 10, without the external compensation capacitor opens the possibility of oscillations near output saturation regions when under load, the improper operation of the thermal shutdown circuit. This can result in amplifier destruction.

At gains of 10 or more:

1. No external components are required.
2. Typical slew rate will be 8V/μs.
3. Typical phase margin will be 20°.

At a gain of 3:

1. Connect a 470pF compensation capacitor between pins 9 and 10.
2. Typical slew rate will be 5V/μs.
3. Typical phase margin will be 45°.

At unity gain:

1. Connect a 1.8nF compensation capacitor between pins 9 and 10.
2. Typical slew rate will be 1.8V/μs.
3. Typical phase margin will be 65°.

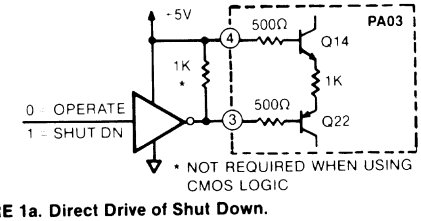



**FIGURE 1a. Direct Drive of Shut Down.**

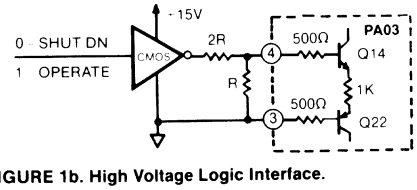



**FIGURE 1b. High Voltage Logic Interface.**

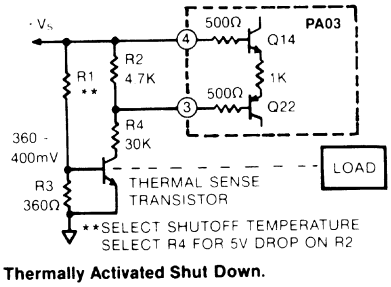



**FIGURE 1c. Thermally Activated Shut Down.**

# PA07 • PA07A

## POWER OPERATIONAL AMPLIFIERS

## FEATURES

- MIL-STD-883C VERSION — PA07M
- LOW BIAS CURRENT — FET Input
- PROTECTED OUTPUT STAGE — Thermal Shutoff
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±12V to ±50V
- HIGH OUTPUT CURRENT — ±5A Peak

## APPLICATIONS

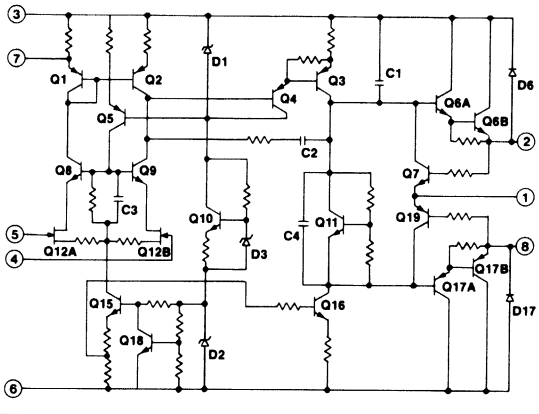
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 100KHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 60W RMS

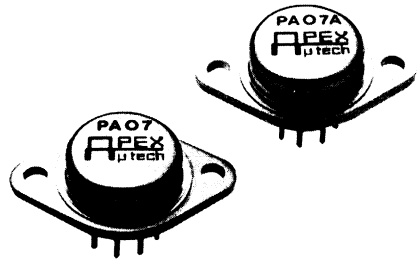
## DESCRIPTION

The PA07 is a high voltage, high output current operational amplifier designed to drive resistive, inductive and capacitive loads. Its complimentary darlington emitter follower output stage is protected against inductive kickback or back EMF. For optimum linearity especially at low levels, the output state is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. A thermal shutoff circuit protects against overheating and minimizes heatsink requirements for abnormal operating conditions. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heat sink of proper rating is recommended.

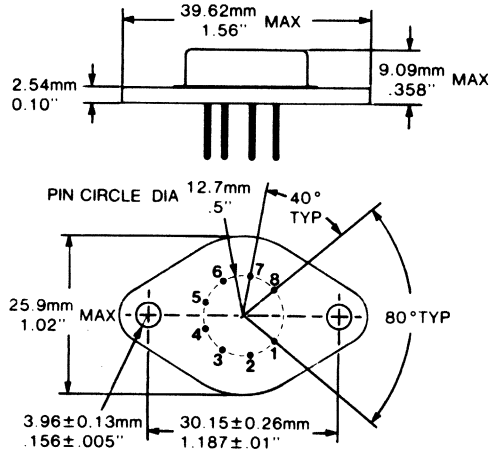
These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is hermetically sealed by one shot resistance welding.

## EQUIVALENT SCHEMATIC



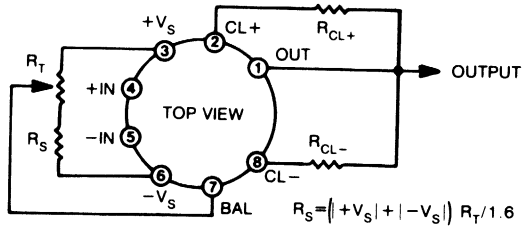




## PACKAGE OUTLINE




| | |
|---|---|
| PIN DIAMETER: | 1.01mm or 0.04" |
| PIN LENGTH: | 10.2mm or 0.40" MIN |
| PIN MATERIAL, STD: | Nickel plated alloy 52, solderable |
| PIN MATERIAL, MIL: | Gold or nickel plated alloy 52, solderable |
| PACKAGE: | Hermetic, nickel plated steel |
| ISOLATION: | 300VDC any pin to case |
| SOCKETS: | APEX PN: MS03 |
| CAGE JACKS: | APEX PN: MS02 (set of 8) |
| HEATSINKS: | APEX PNs: HS01 thru HS05 |

## EXTERNAL CONNECTIONS




NOTE: Input offset voltage trim optional. $R_T = 10K\Omega$ MAX

# PA07 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 100V |
| OUTPUT CURRENT, source | 5A |
| OUTPUT CURRENT, sink | see SOA |
| POWER DISSIPATION, internal[1] | 67W |
| INPUT VOLTAGE, differential | ±50V |
| INPUT VOLTAGE, common-mode | $\pm V_S$ |
| TEMPERATURE, pin solder-10s | 300°C |
| TEMPERATURE, junction[1] | 200°C |
| TEMPERATURE RANGE, storage | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −55 to +125°C |

# SPECIFICATIONS

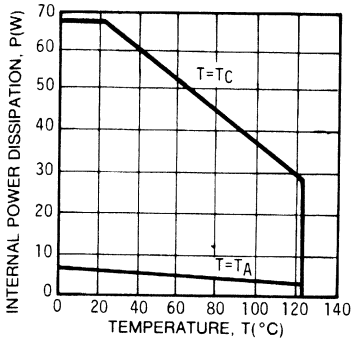
| | | PA07 | | | PA07A | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[2]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C$ = 25°C | | .5 | ±2 | | ±.25 | ±.5 | mV |
| OFFSET VOLTAGE, vs. temperature | Full temperature range | | 10 | 30 | | 5 | 10 | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C$ = 25°C | | 8 | | | * | | µV/V |
| OFFSET VOLTAGE, vs. power | Full temperature range | | 20 | | | 10 | | µV/W |
| BIAS CURRENT, initial[3] | $T_C$ = 25°C | | 5 | 50 | | 3 | 10 | pA |
| BIAS CURRENT, vs. supply | $T_C$ = 25°C | | .01 | | | * | | pA/V |
| OFFSET CURRENT, initial[3] | $T_C$ = 25°C | | 2.5 | 50 | | 1.5 | 10 | pA |
| INPUT IMPEDANCE, dc | $T_C$ = 25°C | | $10^{11}$ | | | * | | Ω |
| INPUT CAPACITANCE | $T_C$ = 25°C | | 4 | | | * | | pF |
| COMMON-MODE VOLTAGE RANGE[4] | Full temperature range | $\pm V_S$ −12 | | | * | | | V |
| COMMON-MODE REJECTION, dc | Full temp. range, $V_{CM}$ = ±20V | | 120 | | | * | | db |
| **GAIN** | | | | | | | | |
| OPEN LOOP GAIN at 10Hz | $T_C$ = 25°C, $R_L$ = 15Ω | 92 | 98 | | * | * | | db |
| GAIN BANDWIDTH PRODUCT at 1MHz | $T_C$ = 25°C, $R_L$ = 15Ω | | 1.3 | | | * | | MHz |
| POWER BANDWIDTH | $T_C$ = 25°C, $R_L$ = 15Ω | | 18 | | | * | | kHz |
| PHASE MARGIN | Full temp. range, $R_L$ = 15Ω | | 70 | | | * | | ° |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[4] | Full temp. range, $I_O$ = 5A | $\pm V_S$ −5 | | | * | | | V |
| VOLTAGE SWING[4] | Full temp. range, $I_O$ = 2A | $\pm V_S$ −5 | | | * | | | V |
| VOLTAGE SWING[4] | Full temp. range, $I_O$ = 90mA | $\pm V_S$ −5 | | | * | | | V |
| CURRENT, peak | $T_C$ = 25°C | 5 | | | * | | | A |
| SETTLING TIME to .1% | $T_C$ = 25°C, 2V step | | 1.5 | | | * | | µs |
| SLEW RATE | $T_C$ = 25°C | | 5 | | | * | | V/µs |
| CAPACITIVE LOAD, unity gain | Full temperature range | | | 10 | | | * | nF |
| CAPACITIVE LOAD, gain>4 | Full temperature range | | | SOA | | | * | |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | Full temperature range | ±12 | ±35 | ±50 | * | * | * | V |
| CURRENT, quiescent | $T_C$ = 25°C | | 18 | 30 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac[5] junction to case | F>60Hz | | 1.9 | 2.1 | | * | * | °C/W |
| RESISTANCE, dc junction to case | F<60Hz | | 2.4 | 2.6 | | * | * | °C/W |
| RESISTANCE, junction to air | | | 30 | | | * | | °C/W |
| TEMPERATURE RANGE, case | Meet full range specification | −25 | 25 | +85 | * | * | * | °C |

**NOTES:** * The specification of PA07A is identical to the specification for PA07 in applicable column to the left.

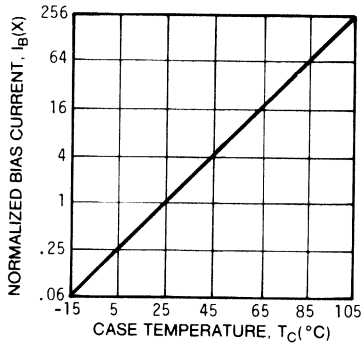
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total $V_S$ is measured from $+V_S$ to $-V_S$.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
7. The PA07M is screened to MIL-STD-883C Class B Method 5008. See military models.

# PA07 TYPICAL PERFORMANCE GRAPHS

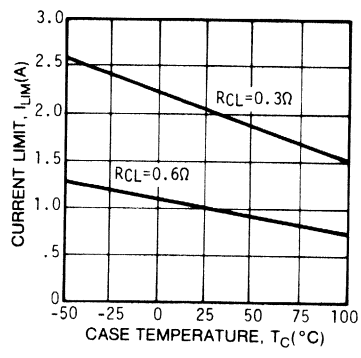
### POWER DERATING



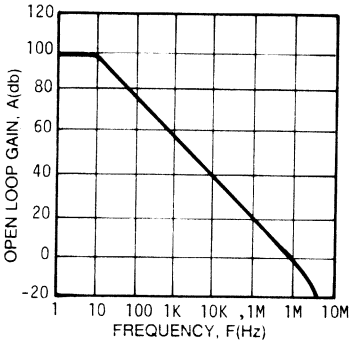

### BIAS CURRENT



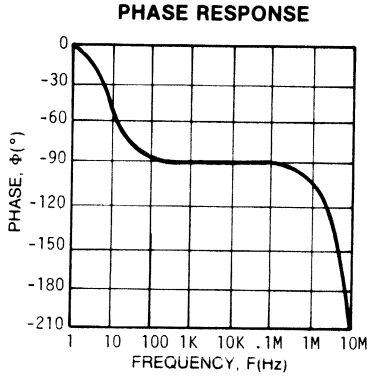

### CURRENT LIMIT



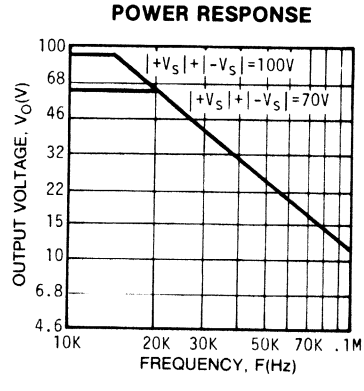

### SMALL SIGNAL RESPONSE



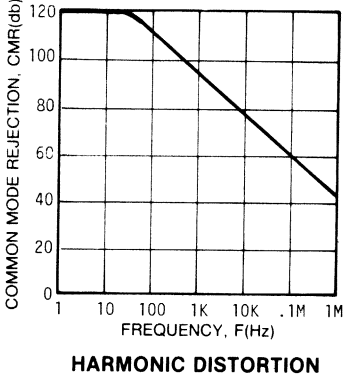

### PHASE RESPONSE



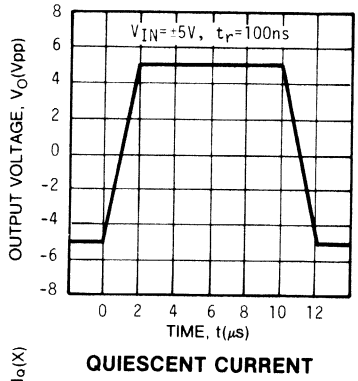

### POWER RESPONSE



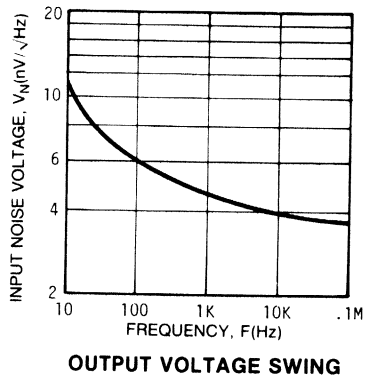

### COMMON MODE REJECTION



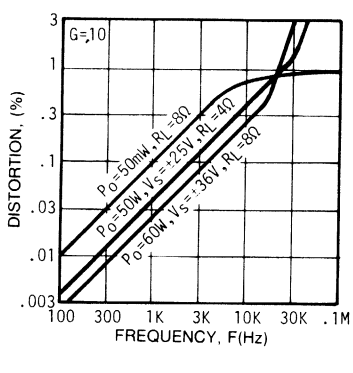

### PULSE RESPONSE



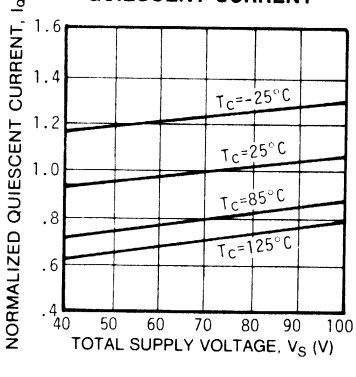

### INPUT NOISE



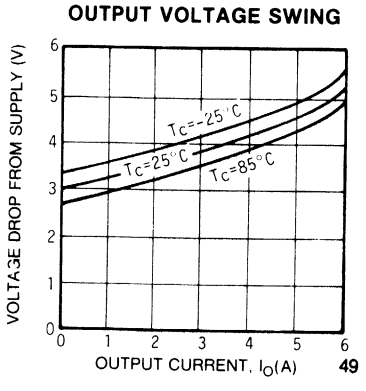

### HARMONIC DISTORTION




### QUIESCENT CURRENT




### OUTPUT VOLTAGE SWING



# PA07 OPERATING CONSIDERATIONS

## GENERAL

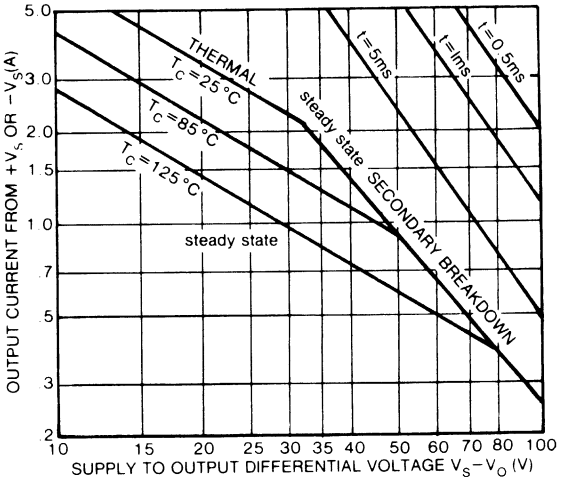
Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks and mating sockets, see the "Package Outline" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

## SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the wire bonds.
2. The secondary breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.

## SAFE OPERATING AREA CURVES




The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximums are safe:

| | CAPACITIVE LOAD | | INDUCTIVE LOAD | |
|---|---|---|---|---|
| $\pm V_S$ | $I_{LIM}$ = 2A | $I_{LIM}$ = 5A | $I_{LIM}$ = 2A | $I_{LIM}$ = 5A |
| 50V | 80μF | 75μF | 55mH | 7.5mH |
| 40V | 250μF | 150μF | 150mH | 11mH |
| 30V | 1,200μF | 500μF | 250mH | 24mH |
| 20V | 20mF | 5mF | 1.5H | 75mH |
| 15V | ∞ | 25mF | ∞ | 100mH |

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 12V below the supply rail with $I_{LIM}$ = 5A or 32V below the supply rail with $I_{LIM}$ = 2A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or shorts to common if the current limits are set as follows at $T_C$ = 25°C.

| $\pm V_S$ | SHORT TO $\pm V_S$, C, L OR EMF LOAD | SHORT TO COMMON |
|---|---|---|
| 50V | .25A | .82A |
| 40V | .37A | 1.4A |
| 30V | .65A | 2.1A |
| 20V | 1.4A | 3.3A |
| 15V | 2.1A | 4.5A |

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

## THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds safe limits. This allows the heatsink design to be based solely on normal conditions but prevents excessive temperatures during abnormal high power conditions without overdesigning the heatsink.

Under abnormal operating conditions, activation of the thermal shutdown is a sign that the internal temperatures have reached approximately 150°. Continued operation in this temperature range will reduce the life of the product. Also, in this operating mode the device may oscillate in and out of thermal shutoff destroying useful signals.

# PA08 • PA08A

## POWER OPERATIONAL AMPLIFIERS

## FEATURES

- MIL-STD-883C VERSION — PA08M
- WIDE SUPPLY RANGE — ±15V to ±150V
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH OUTPUT CURRENT — Up to ±150mA
- LOW BIAS CURRENT — FET Input
- PROTECTED OUTPUT STAGE — Thermal Shutoff

## APPLICATIONS

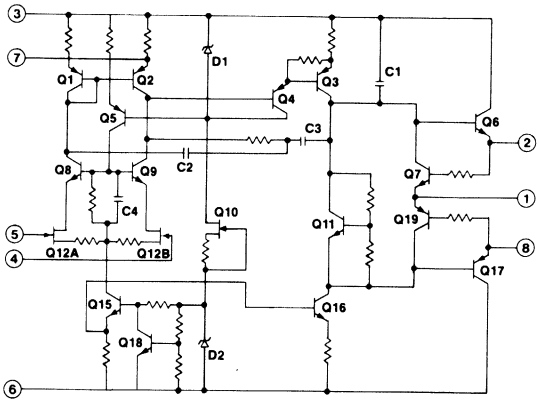
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 290V
- ANALOG SIMULATION

## DESCRIPTION

The PA08 is a high voltage operational amplifier designed for output voltage swings of up to ±145V with a dual (±) supply or 290V with a single supply. High accuracy is achieved with a cascade input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA08 features an unprecedented supply range and excellent supply rejection. The output stage is biased-on for linear operation. Internal phase compensation assures stability at all gain settings. The safe operating area (SOA) can be observed with all types of loads by choosing the appropriate current limiting resistors. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A built-in thermal shutoff circuit prevents destructive overheating. However, a heatsink may be necessary to maintain the proper case temperature under nornal operating conditions.

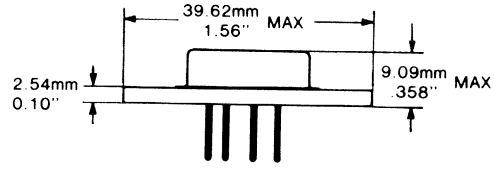
These hybrid integrated circuits utilize beryllia (BeO) substrates, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is hermetically sealed by one shot resistance welding.

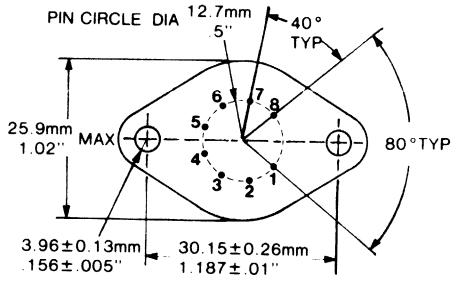
## EQUIVALENT SCHEMATIC





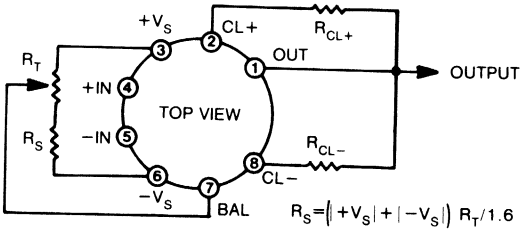

## PACKAGE OUTLINE




| | |
|---|---|
| PIN DIAMETER: | 1.01mm or 0.04" |
| PIN LENGTH: | 10.2mm or 0.40" MIN |
| PIN MATERIAL, STD: | Nickel plated alloy 52, solderable |
| PIN MATERIAL, MIL: | Gold or nickel plated alloy 52, solderable |
| PACKAGE: | Hermetic, nickel plated steel |
| ISOLATION: | 300VDC any pin to case |
| SOCKETS: | APEX PN: MS03 |
| CAGE JACKS: | APEX PN: MS02 (set of 8) |
| HEATSINKS: | APEX PNs: HS01 thru HS05 |

## EXTERNAL CONNECTIONS




NOTE: Input offset voltage trim optional. $R_T$=10KΩ MAX

# PA08 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 300V |
| OUTPUT CURRENT, source | 200mA |
| OUTPUT CURRENT, sink | see SOA |
| POWER DISSIPATION, internal at $T_C = 25°C$ | 17.5W |
| INPUT VOLTAGE, differential | ±50V |
| INPUT VOLTAGE, common-mode | $\pm V_S$ |
| TEMPERATURE, pin solder-10s max | 300°C |
| TEMPERATURE, junction[1] | 200°C |
| TEMPERATURE RANGE, storage | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −55 to +125°C |

# SPECIFICATIONS

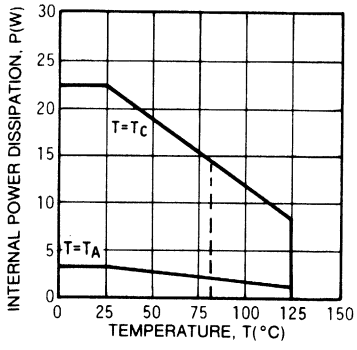
| | | PA08 | | | PA08A | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[2]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C = 25°C$ | | ±.5 | ±2 | | ±.25 | ±.5 | mV |
| OFFSET VOLTAGE, vs. temperature | $T_C = -25$ to $+85°C$ | | ±15 | ±30 | | ±5 | ±10 | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C = 25°C$ | | ±.5 | | | * | 2 | µV/V |
| OFFSET VOLTAGE, vs. time | $T_C = 25°C$ | | ±75 | | | * | | µV/√kh |
| BIAS CURRENT, initial[3] | $T_C = 25°C$ | | 5 | 50 | | 3 | 10 | pA |
| BIAS CURRENT, vs. supply | $T_C = 25°C$ | | .01 | | | * | | pA/V |
| OFFSET CURRENT, initial[3] | $T_C = 25°C$ | | ±2.5 | ±50 | | ±1.5 | ±10 | pA |
| INPUT IMPEDANCE, dc | $T_C = 25°C$ | | $10^5$ | | | * | | MΩ |
| INPUT CAPACITANCE | $T_C = 25°C$ | | 4 | | | * | | pF |
| COMMON-MODE VOLTAGE RANGE[4] | $T_C = -25$ to $+85°C$ | $\pm V_S - 10$ | | | * | | | V |
| COMMON-MODE REJECTION, dc | $T_C = -25°C$ to $+85°C$, $V_{CM} = \pm 90V$ | | 130 | | | * | | db |
| **GAIN** | | | | | | | | |
| OPEN LOOP GAIN at 10Hz | $T_C = 25°C$, $R_L = \infty$ | | 118 | | | * | | db |
| OPEN LOOP GAIN at 10Hz | $T_C = 25°C$, $R_L = 1.2K\Omega$ | 96 | 111 | | * | * | | db |
| GAIN BANDWIDTH PRODUCT at 1MHz | $T_C = 25°C$, $R_L = 1.2K\Omega$ | | 5 | | | * | | MHz |
| POWER BANDWIDTH | $T_C = 25°C$, $R_L = 1.2K\Omega$ | | 90 | | | * | | kHz |
| PHASE MARGIN | $T_C = -25$ to $+85°C$ | | 60 | | | * | | ° |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[4] | $T_C = 25°C$, $I_O = 150mA$ | $\pm V_S - 15$ | $\pm V_S - 8$ | | * | * | | V |
| VOLTAGE SWING[4] | $T_C = -25°C$ to $+85°C$, $I_O = \pm 75mA$ | $\pm V_S - 10$ | $\pm V_S - 5$ | | * | * | | V |
| VOLTAGE SWING[4] | $T_C = -25°C$ to $+85°C$, $I_O = \pm 20mA$ | $\pm V_S - 5$ | $\pm V_S - 3$ | | * | * | | V |
| CURRENT, peak | $T_C = 85°C$ | 150 | | | * | | | mA |
| SLEW RATE | $T_C = 25°C$ | | 30 | | 20 | * | | V/µs |
| CAPACITIVE LOAD, G = 1 | $T_C = -25$ to $+85°C$ | | | 10 | | | * | nF |
| CAPACITIVE LOAD, G > 4 | $T_C = -25$ to $+85°C$ | | | SOA | | | * | |
| SETTLING TIME to .1% | $T_C = 25°C$, $R_L = 1.2K\Omega$, 2V step | | 1 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | $T_C = -55$ to $+125°C$ | ±15 | ±100 | ±150 | * | * | * | V |
| CURRENT, quiescent | $T_C = 25°C$ | | 6 | 8.5 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac junction to case[5] | $T_C = -55$ to $+125°C$, F>60Hz | | 3.8 | | | * | | °C/W |
| RESISTANCE, dc junction to case | $T_C = -55$ to $+125°C$, F<60Hz | | 6.0 | 6.5 | | * | * | °C/W |
| RESISTANCE, junction to air | $T_C = -55$ to $+125°C$ | | 30 | | | * | | °C/W |

**NOTES:** * The specification of PA08A is identical to the specification for PA08 in applicable column to the left.

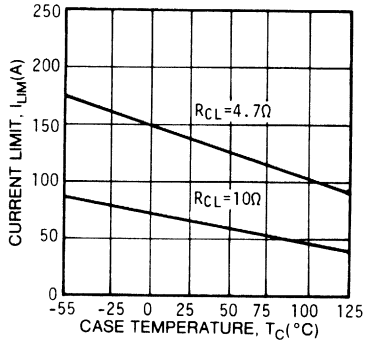
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. The power supply voltage specified under typical (TYP) applies unless otherwise noted.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies only if output current alternates between both output transistors at a rate faster than 60Hz.
6. The internal substrate contains beryllia (BeO). Do not break the hermetic seal. If broken do not crush, machine, or subject to temperatures over 850°C to avoid generating toxic (Be) fumes.
7. The PA08M is screened to MIL-STD-883C Class B Method 5008. See military models.

# PA08 TYPICAL PERFORMANCE GRAPHS

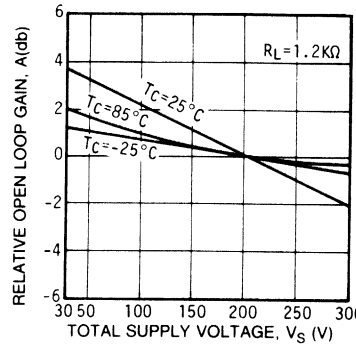
### POWER DERATING



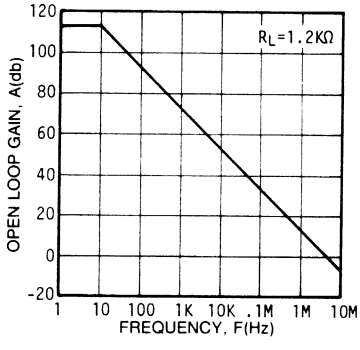

### CURRENT LIMIT



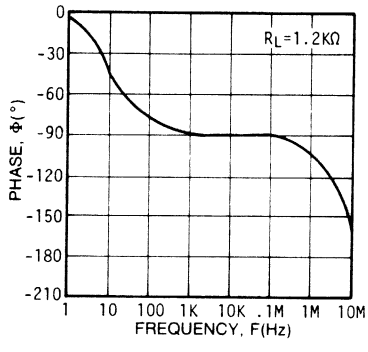

### OPEN LOOP GAIN



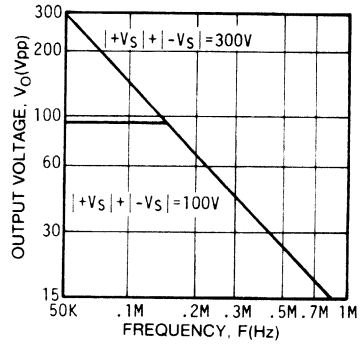

### SMALL SIGNAL RESPONSE



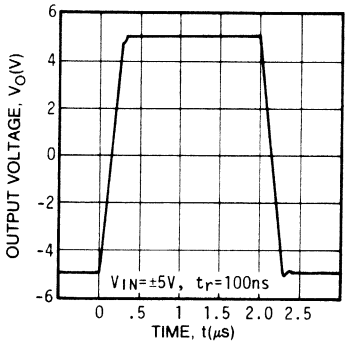

### PHASE RESPONSE



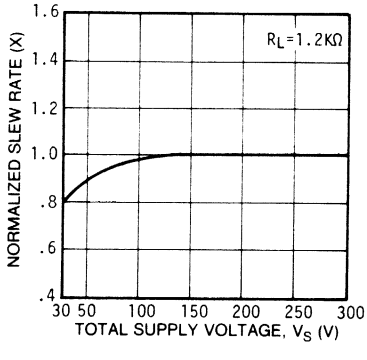

### POWER RESPONSE



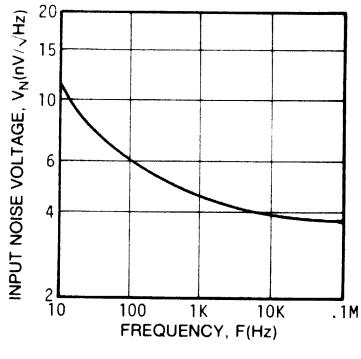

### PULSE RESPONSE



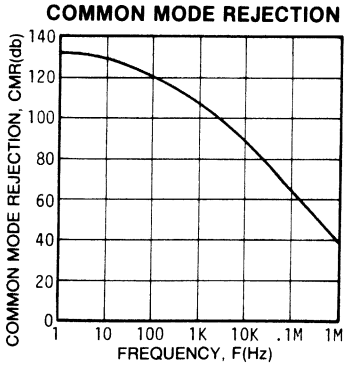

### SLEW RATE



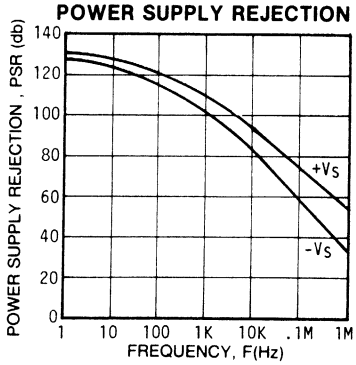

### INPUT NOISE



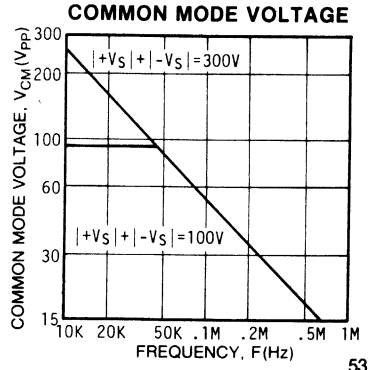

### COMMON MODE REJECTION




### POWER SUPPLY REJECTION




### COMMON MODE VOLTAGE



# PA08 OPERATING CONSIDERATIONS

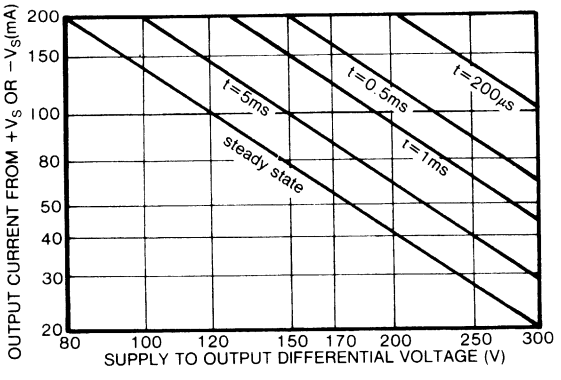
## GENERAL

Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks, and mating sockets, see the "Package Outlines" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

## SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The secondary breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.




The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. Under transient conditions, the following capacitive and inductive loads are safe with the current limits set to the maximum:

| ±$V_S$ | C(MAX) | L(MAX) |
|---|---|---|
| 150V | .4µF | 280mH |
| 125V | .9µF | 380mH |
| 100V | 2µF | 500mH |
| 75V | 10µF | 1200mH |
| 50V | 100µF | 13H |

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or simple shorts to common if the current limits are set as follows:

| ±$V_S$ | SHORT TO ±$V_{SC}$, C, L or EMF LOAD | SHORT TO COMMON |
|---|---|---|
| 150V | 20mA | 67mA |
| 125V | 27mA | 90mA |
| 100V | 42mA | 130mA |
| 75V | 67mA | 200mA |
| 50V | 130mA | 200mA |

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

## THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds safe limits. This allows the heatsink design to be based solely on normal conditions but prevents excessive temperatures during abnormal high power conditions without overdesigning the heatsink.

Under abnormal operating conditions, activation of the thermal shutdown is a sign that the internal temperatures have reached approximately 150°. Continued operation in this temperature range will reduce the life of the product. Also, in this operating mode the device may oscillate in and out of thermal shutoff destroying useful signals.

## INDUCTIVE LOADS

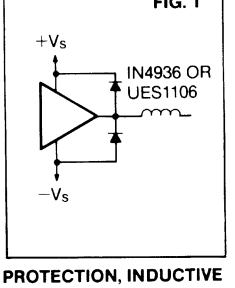
Two external diodes as shown in figure 2, are required to protect these amplifiers flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

## INPUT PROTECTION

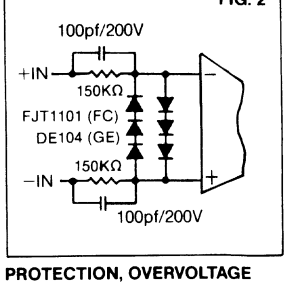
The input is protected against common mode voltages up to the supply rails and differential voltages up to ±50V. Increased protection against differential input voltages can be obtained by adding 2 resistors, 2 capacitors and 6 low leakage diodes as shown in figure 2.

FIG. 1




PROTECTION, INDUCTIVE LOAD

FIG. 2




PROTECTION, OVERVOLTAGE

# PA09 • PA09A

## FEATURES

- V-MOS TECHNOLOGY — 4A peak rating
- HIGH GAIN BANDWIDTH PRODUCT — 150MHz
- VERY FAST SLEW RATE — 400$\mu$s
- PROTECTED OUTPUT STAGE — Thermal Shutoff
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±40V
- LOW BIAS CURRENT, LOW NOISE — FET Input

## APPLICATIONS

- VIDEO DISTRIBUTION AND AMPLIFICATION
- HIGH SPEED DEFLECTION CIRCUITS
- POWER TRANSDUCERS UP TO 5MHz
- COAXIAL LINE DRIVERS
- POWER LED OR LASER DIODE EXCITATION

## DESCRIPTION

The PA09 is a high voltage, high current operational amplifier optimized to drive a variety of loads from DC through the video frequency range. Excellent input accuracy is achieved with a dual monolythic FET input transistor which is cascaded by two high voltage transistors to provide outstanding common mode characteristics. All internal current and voltage levels are referenced to a zener diode biased on by a current source. As a result, the PA09 exhibits superior DC and AC stability over a wide supply and temperature range.

High speed and freedom from secondary breakdown is assured by a complimentary V-MOS output stage. For optimum linearity, especially at low levels, the V-MOS transistors are biased in the class A/B mode. Thermal shutoff provides full protection against overheating and limits the heatsink requirements to dissipate the internal power losses under normal operating conditions. A built-in current limit protects the amplifier against overloading. Inductive load kickback protection is provided by two internal clamping diodes. External phase compensation allows the user maximum flexibility in obtaining the optimum slew rate and gain bandwidth product at all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnection at all operating temperatures. The 8 pin TO-3 package is hermetically sealed by resistance welding.

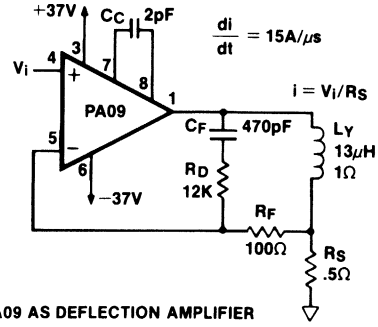
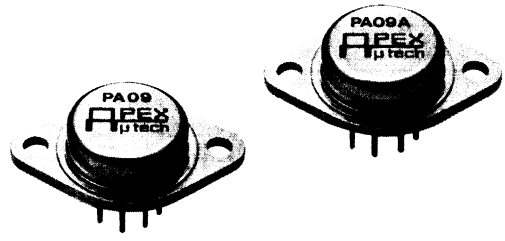
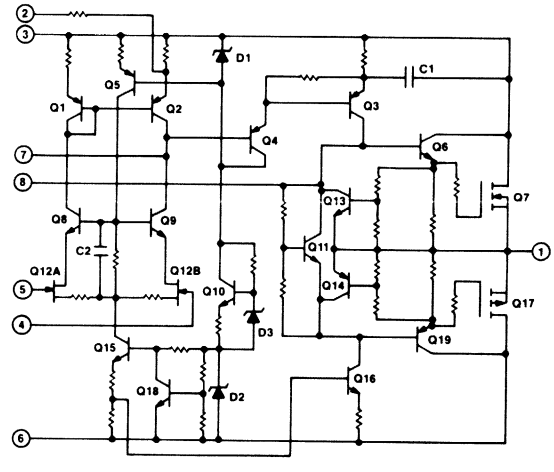


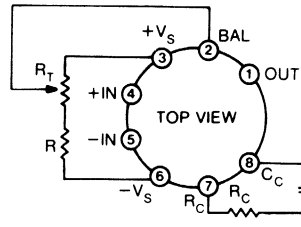

FIG 1: PA09 AS DEFLECTION AMPLIFIER




## EQUIVALENT SCHEMATIC




## EXTERNAL CONNECTIONS




**PHASE COMPENSATION**

| GAIN | $C_C$ | $R_C$ |
|---|---|---|
| 1 | 100pf | 200Ω |
| 10 | 15pf | 0Ω |
| 100 | 5pf | 0Ω |
| 1000 | none | none |

$R = (|+V_S| + |-V_S|)\, R_T / 1.6$

NOTE: Input offset voltage trim optional $R_T$ = 10KΩ MAX

# PA09 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 80V |
| OUTPUT CURRENT, source | 5A |
| OUTPUT CURRENT, sink | see SOA |
| POWER DISSIPATION, internal[1] | 78W |
| INPUT VOLTAGE, differential | 40V |
| INPUT VOLTAGE, common-mode | $\pm V_S$ |
| TEMPERATURE, pin solder-10s | 300°C |
| TEMPERATURE, junction[1] | 150°C |
| TEMPERATURE RANGE, storage | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −55 to +125°C |

# SPECIFICATIONS

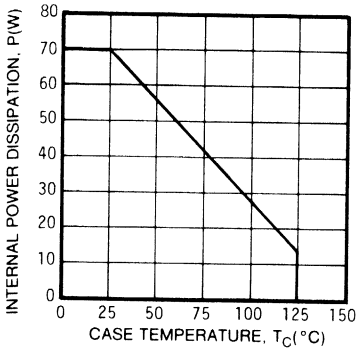
| | | PA09 | | | PA09A | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[2]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C$ = 25°C | | .5 | ±3 | | ±.25 | ±.5 | mV |
| OFFSET VOLTAGE, vs. temperature | $T_C$ = 25°C to +85°C | | 10 | 30 | | 5 | 10 | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C$ = 25°C | | 10 | | | * | | µV/V |
| OFFSET VOLTAGE, vs. power | $T_C$ = 25°C to +85°C | | 20 | | | * | | µV/W |
| BIAS CURRENT, initial | $T_C$ = 25°C | | 5 | 100 | | 3 | 20 | pA |
| BIAS CURRENT, vs. supply | $T_C$ = 25°C | | .01 | | | * | | pA/V |
| OFFSET CURRENT, initial | $T_C$ = 25°C | | 2.5 | 50 | | 1.5 | 10 | pA |
| INPUT IMPEDANCE, dc | $T_C$ = 25°C | | $10^{11}$ | | | * | | Ω |
| INPUT CAPACITANCE | $T_C$ = 25°C | | 6 | | | * | | pF |
| COMMON-MODE VOLT. RANGE[3] | $T_C$ = −25°C to +85°C | $\pm V_S$ −10 | $\pm V_S$ −8 | | * | * | | V |
| COMMON-MODE REJECTION, dc | $T_C$ = −25°C to +85°C, $V_{CM}$=±20V | | 104 | | | * | | db |
| **GAIN** | | | | | | | | |
| OPEN LOOP GAIN at 10Hz | $T_C$ = 25°C, $R_L$ = 1kΩ | | 90 | | | * | | db |
| OPEN LOOP GAIN at 10Hz | $T_C$ = 25°C, $R_L$ = 15Ω | 80 | 88 | | * | * | | db |
| GAIN BANDWIDTH PRODUCT at 1MHz | $T_C$ = 25°C, $R_L$ = 15Ω, $C_C$ = 5pF | | 150 | | | * | | MHz |
| POWER BANDWIDTH, high gain | $T_C$ = 25°C, $R_L$ = 15Ω, $C_C$ = 5pF | | 1.2 | | | * | | MHz |
| POWER BANDWIDTH, low gain | $T_C$ = 25°C, $R_L$ = 15Ω, $C_C$=100pF | | .75 | | | * | | MHz |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[3] | $T_C$ = −25°C to +85°C, $I_O$ = 2A | $\pm V_S$ −8 | $\pm V_S$ −7 | | * | * | | V |
| CURRENT, short circuit | $T_C$ = 25°C | | 4.5 | | | * | | A |
| SETTLING TIME to .1% | $T_C$ = 25°C, 2V step | | .3 | | | * | | µs |
| SETTLING TIME to .01% | $T_C$ = 25°C, 2V step | | 1.2 | | | * | | µs |
| SLEW RATE, high gain | $T_C$ = 25°C, $C_C$ = 5pF | | 400 | | | * | | V/µs |
| SLEW RATE, low gain | $T_C$ = 25°C, $C_C$ = 100pF | | 75 | | | * | | V/µs |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | $T_C$ = −25°C to +85°C | ±12 | ±35 | ±40 | * | * | * | V |
| CURRENT, quiescent | $T_C$ = 25°C | | 70 | 85 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac junction to case[4] | $T_C$ = −25°C to +85°C, F>60Hz | | 1.2 | 1.3 | | * | * | °C/W |
| RESISTANCE, dc junction to case | $T_C$ = −25°C to +85°C, F<60Hz | | 1.6 | 1.8 | | * | * | °C/W |
| RESISTANCE, junction to air | $T_C$ = −25°C to +85°C | | 30 | | | * | | °C/W |

**NOTES:** * The specification of PA09A is identical to the specification for PA09 in applicable column to the left.

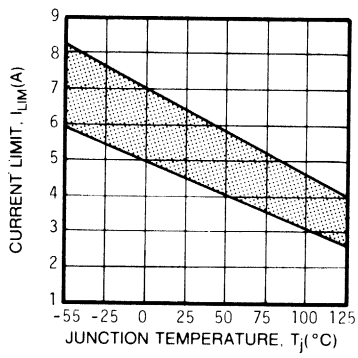
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±35V unless otherwise specified as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total $V_S$ is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
6. The PA09M is screened to MIL-STD-883C Class B Method 5008. See Military Models.

# PA09 TYPICAL PERFORMANCE GRAPHS

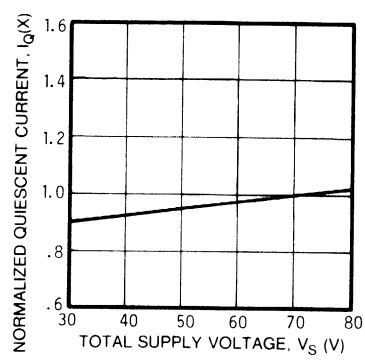
### POWER DERATING



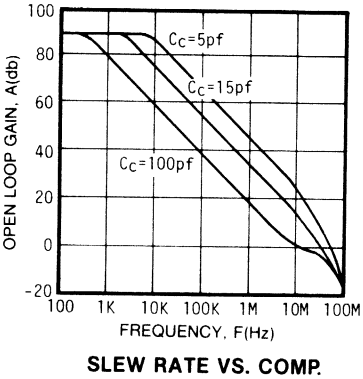

### CURRENT LIMIT



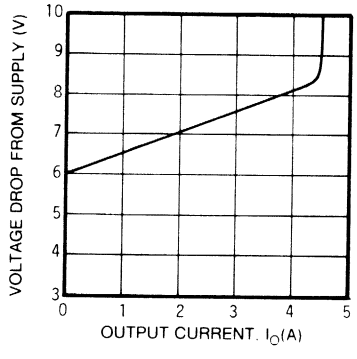

### QUIESCENT CURRENT



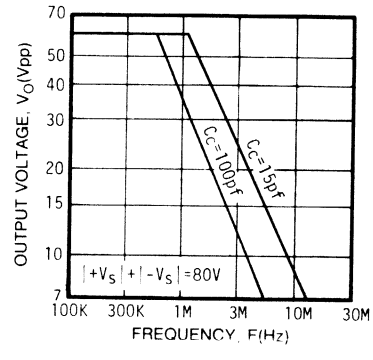

### SMALL SIGNAL RESPONSE



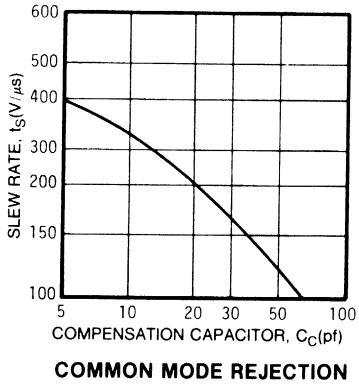

### OUTPUT VOLTAGE SWING



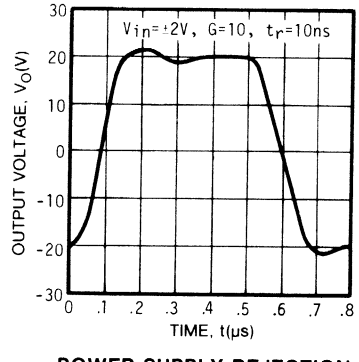

### POWER RESPONSE



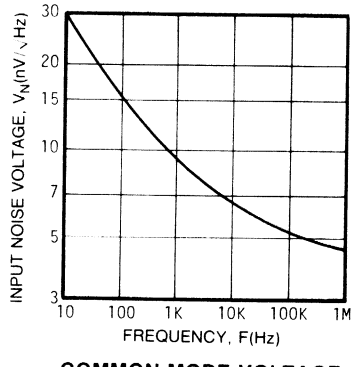

### SLEW RATE VS. COMP.



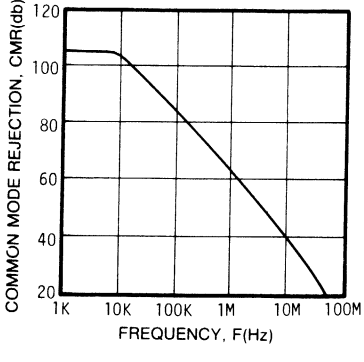

### PULSE RESPONSE



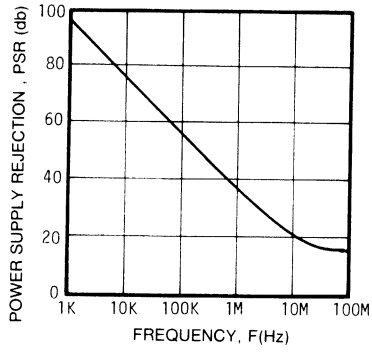

### INPUT NOISE



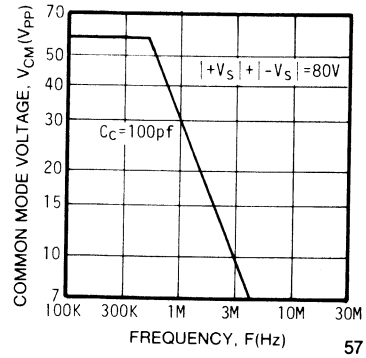

### COMMON MODE REJECTION




### POWER SUPPLY REJECTION




### COMMON MODE VOLTAGE



# PA09 OPERATING CONSIDERATIONS

## GENERAL

Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks, and mating sockets, see the "Package Outlines" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

## DEFECTION AMPLIFIER (FIG. 1)

The deflection amplifier circuit on the first page of this data sheet achieves arbitrary beam positioning for a fast heads up display. Maximum transition times are 4$\mu$s while delivering 2A pk currents to the 13mH coil. The key to this circuit is the sense resistor ($R_S$) which converts yoke current to voltage for op amp feedback. This negative feedback forces the coil current to stay exactly proportional to the control voltage. The network consisting of $R_d$, $R_f$ and $C_f$ serves to shift from a current feedback via $R_S$ to a direct voltage feedback at the upper frequencies. This removes the extra phase shift caused by the inductor thus preventing oscillation. See Application Note 5 for details of this and other precision magnetic deflection circuits.

## SUPPLY VOLTAGE

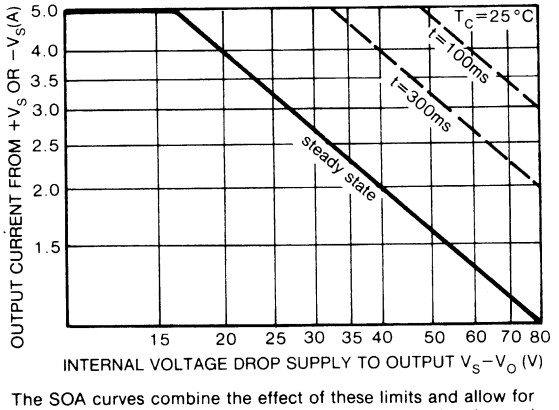
The specified voltage ($\pm V_S$) applies for a dual ($\pm$) supply having equal voltages. A nonsymmetrical (ie. +70/−10V) or a single supply (ie. 80V) may be used as long as the total voltage between the $+V_S$ and $-V_S$ rails does not exceed the sum of the voltages of the specified dual supply.

## SAFE OPERATING AREA (SOA)

The output stage of these V-MOS power op amps has 2 distinct limitations:

1. The current handling capability of the wire bonds.
2. The junction temperature of the output transistors.

### SAFE OPERATING AREA CURVES




The SOA curves combine the effect of these limits and allow for internal thermal delays. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

1. Capacitive and inductive loads up to the following maximums are safe:

| $\pm V_S$ | CAPACITIVE LOAD | INDUCTIVE LOAD |
|---|---|---|
| 40V | .1$\mu$F | 11mH |
| 30V | 500$\mu$F | 24mH |
| 20V | 2500$\mu$F | 75mH |
| 15V | $\infty$ | 100mH |

2. Short circuits to ground are safe with dual supplies up to $\pm$20V.

## BYPASSING OF SUPPLIES

Each supply rail must be bypassed to common with a tantalum capacitor of at least 47$\mu$F in parallel with a .47$\mu$F ceramic capacitor directly connected from the power supply pins to the ground plane.

## OUTPUT LEADS

Keep the output leads as short as possible. In the video frequency range, even a few inches of wire have significant inductance, raising the interconnection impedance and limiting the output current slew rate. Futhermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.

## GROUNDING

Single point grounding of the input resistors and the input signal to a common ground plane will prevent undesired current feedback, which can cause large errors and/or instabilities.

## THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds safe limits. This allows the heatsink design to be based solely on normal conditions but prevents excessive temperatures during abnormal high power conditions without overdesigning the heatsink.

Under abnormal operating conditions, activation of the thermal shutdown is a sign that the internal temperatures have reached approximately 150°. Continued operation in this temperature range will reduce the life of the product. Also, in this operating mode the device may oscillate in and out of thermal shutoff destroying useful signals.

## STABILITY

Due to its large bandwidth the PA09 is more likely to oscillate than lower bandwidth Power Operational Amplifiers. To prevent oscillations a reasonable phase margin must be maintained by:

1. Selection of the proper phase compensation capacitor and resistor. Use the values given in the table under external connections on Page 1 and interpolate if necessary. The phase margin can be increased by using a large capacitor and a smaller resistor than the slew rate optimized values listed in the table.
2. Keeping the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistances can be used with increased phase compensation and/or bypassing of the feedback resistor.
3. Connect the case to a local AC ground potential.

# PA10 • PA10A

## POWER OPERATIONAL AMPLIFIERS

## FEATURES

- MIL-STD-883C VERSION — PA10M
- GAIN BANDWIDTH PRODUCT — 6MHz
- TEMP. RANGE — -55 to +125°C (PA10A)
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±50V
- HIGH OUTPUT CURRENT — ±5A Peak

## APPLICATIONS

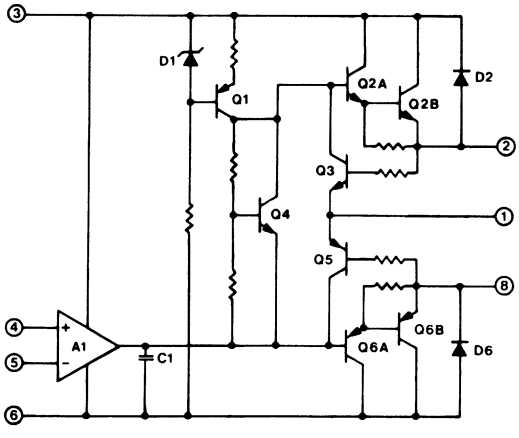
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 100KHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 60W RMS

## DESCRIPTION

The PA10 and PA10A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complimentary darlington emitter follower output stages are protected against inductive kickback or back EMF. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heat sink of proper rating is recommended.

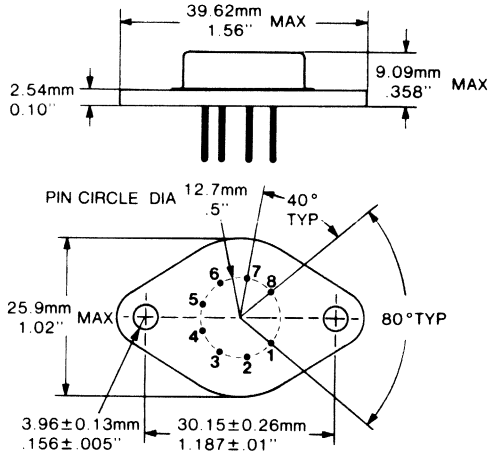
These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is hermetically sealed by one shot resistance welding.

## EQUIVALENT SCHEMATIC



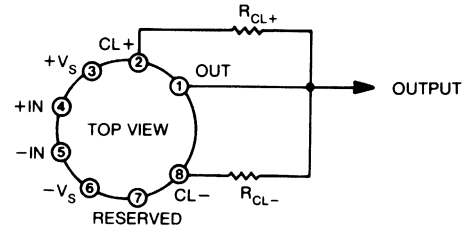



## PACKAGE OUTLINE




| | |
|---|---|
| PIN DIAMETER: | 1.01mm or .04" |
| PIN LENGTH: | 10.2mm or .40" MIN |
| PIN MATERIAL STD: | Nickel plated alloy 52, solderable |
| PIN MATERIAL MIL: | Gold plated alloy 52, solderable |
| PACKAGE: | Hermetic, nickel plated steel |
| ISOLATION: | 300VDC any pin to case |
| SOCKET: | 8 PIN TO-3, APEX PN: MS03 |
| HEATSINKS: | 8 PIN TO-3, APEX PN: HS01 thru HS05 |

## EXTERNAL CONNECTIONS



# PA10 ABSOLUTE MAXIMUM RATINGS

| | PA10 | PA10A |
|---|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 100V | 100V |
| OUTPUT CURRENT, source | 5A | 5A |
| OUTPUT CURRENT, sink | see SOA | see SOA |
| POWER DISSIPATION, internal | 67W | 67W |
| INPUT VOLTAGE, differential | $\pm V_S$ −3V | $\pm V_S$ −3V |
| INPUT VOLTAGE, common-mode | $\pm V_S$ | $\pm V_S$ |
| TEMPERATURE, pin solder-10s | 300°C | 300°C |
| TEMPERATURE, junction[1] | 200°C | 200°C |
| TEMPERATURE RANGE, storage | −65 to +150°C | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −55 to +100°C | −55 to +125°C |

# SPECIFICATIONS

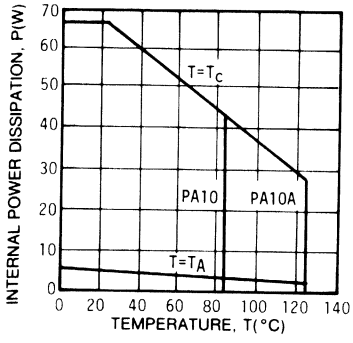
| | | PA10 | | | PA10A | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[2]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C$ = 25°C | | ±2 | ±6 | | ±1 | ±3 | mV |
| OFFSET VOLTAGE, vs. temperature | Full temperature range | | ±10 | ±65 | | * | ±40 | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C$ = 25°C | | ±30 | ±200 | | * | * | µV/V |
| OFFSET VOLTAGE, vs. power | $T_C$ = 25°C | | ±20 | | | * | | µV/W |
| BIAS CURRENT, initial | $T_C$ = 25°C | | 12 | 30 | | 10 | 20 | nA |
| BIAS CURRENT, vs. temperature | Full temperature range | | ±50 | ±400 | | * | * | pA/°C |
| BIAS CURRENT, vs. supply | $T_C$ = 25°C | | ±10 | | | * | | pA/V |
| OFFSET CURRENT, initial | $T_C$ = 25°C | | ±12 | ±30 | | ±5 | ±10 | nA |
| OFFSET CURRENT, vs. temperature | Full temperature range | | ±50 | | | * | | pA/°C |
| INPUT IMPEDANCE, dc | $T_C$ = 25°C | | 200 | | | * | | MΩ |
| INPUT CAPACITANCE | $T_C$ = 25°C | | 3 | | | * | | pF |
| COMMON-MODE VOLTAGE RANGE[3] | Full temperature range | $\pm V_S$ −5 | $\pm V_S$ −3 | | * | * | | V |
| COMMON-MODE REJECTION, dc[3] | Full temp. range, $V_{CM}$ = $\pm V_S$ −6V | 74 | 100 | | * | * | | db |
| **GAIN** | | | | | | | | |
| OPEN LOOP GAIN at 10Hz | $T_C$ = 25°C, 1KΩ load | | 110 | | | * | | db |
| OPEN LOOP GAIN at 10Hz | Full temp. range, 15Ω load | 96 | 108 | | * | * | | db |
| GAIN BANDWIDTH PRODUCT at 1MHz | $T_C$ = 25°C, 15Ω load | | 6 | | | * | | MHz |
| POWER BANDWIDTH | $T_C$ = 25°C, 15Ω load | 15 | 23 | | * | * | | kHz |
| PHASE MARGIN | Full temp. range, 15Ω load | | 20 | | | * | | ° |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[3] | $T_C$ = 25°C, $I_O$ = 5A | $\pm V_S$ −8 | $\pm V_S$ −5 | | $\pm V_S$ −6 | * | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 2A | $\pm V_S$ −6 | | | * | | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 80mA | $\pm V_S$ −5 | | | * | | | V |
| CURRENT, peak | $T_C$ = 25°C | 5 | | | * | | | A |
| SETTLING TIME to .1% | $T_C$ = 25°C, 2V step | | 2 | | | * | | µs |
| SLEW RATE | $T_C$ = 25°C | 2.5 | 5 | | * | * | | V/µs |
| CAPACITIVE LOAD | Full temp. range, G = 1 | | | 1.5 | | | * | nF |
| CAPACITIVE LOAD | Full temp. range, G > 10 | | | SOA | | | * | |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | Full temperature range | ±10 | ±40 | ±45 | * | * | ±50 | V |
| CURRENT, quiescent | $T_C$ = 25°C | 8 | 15 | 30 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac[4] junction to case | $T_C$ = −55 to +125°C, F>60Hz | | 1.9 | 2.1 | | * | * | °C/W |
| RESISTANCE, dc junction to case | $T_C$ = −55 to +125°C | | 2.4 | 2.6 | | * | * | °C/W |
| RESISTANCE, junction to air | $T_C$ = −55 to +125°C | | 30 | | | * | | °C/W |
| TEMPERATURE RANGE[6], case | Specified as full range | −25 | | +85 | −55 | | +125 | °C |

**NOTES:** * The specification of PA10A is identical to the specification for PA10 in applicable column to the left.

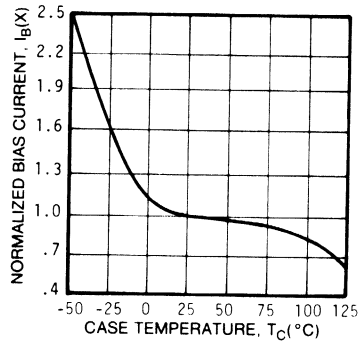
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±40 otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total $V_S$ is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
6. The PA10M is screened to MIL-STD-883C Class B Method 5008. See military models.

# PA10 TYPICAL PERFORMANCE GRAPHS

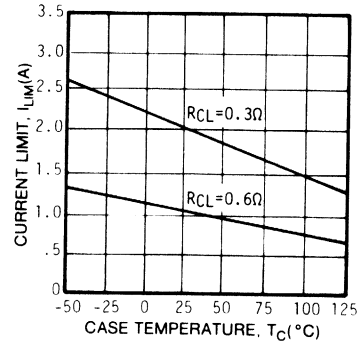
### POWER DERATING



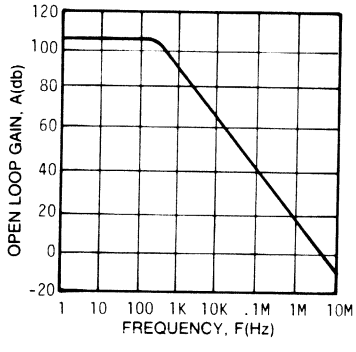

### BIAS CURRENT



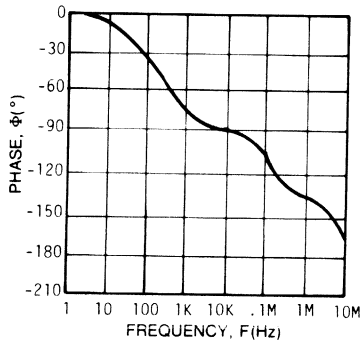

### CURRENT LIMIT



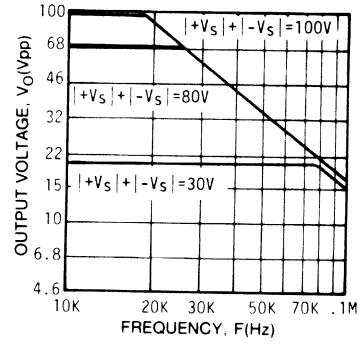

### SMALL SIGNAL RESPONSE



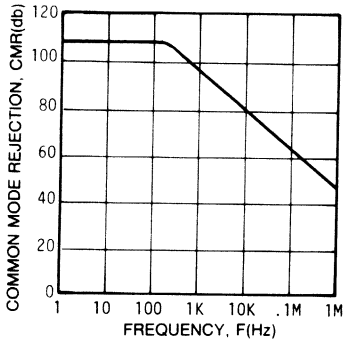

### PHASE RESPONSE



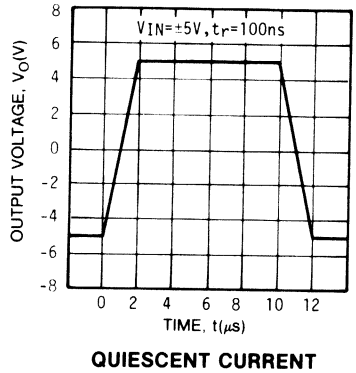

### POWER RESPONSE



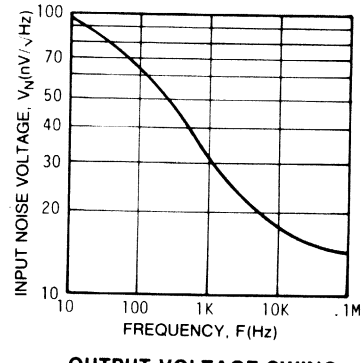

### COMMON MODE REJECTION



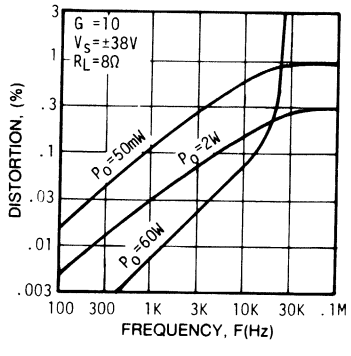

### PULSE RESPONSE



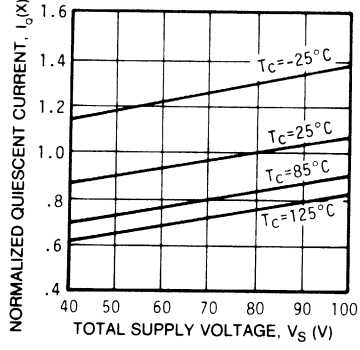

### INPUT NOISE



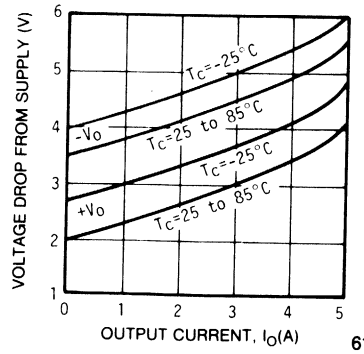

### HARMONIC DISTORTION




### QUIESCENT CURRENT




### OUTPUT VOLTAGE SWING



# PA10 OPERATING CONSIDERATIONS

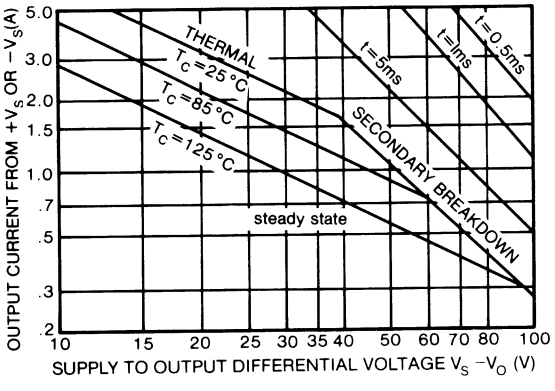
## GENERAL

Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks, and mating sockets, see the "Package Outlines" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

## SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The secondary breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.




The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified:

| | CAPACITIVE LOAD | | INDUCTIVE LOAD | |
|---|---|---|---|---|
| $\pm V_S$ | $I_{LIM}$ = 2A | $I_{LIM}$ = 5A | $I_{LIM}$ = 2A | $I_{LIM}$ = 5A |
| 50V | 80μF | 75μF | 55mH | 7.5mH |
| 40V | 250μF | 150μF | 150mH | 11mH |
| 35V | 500μF | 250μF | 200mH | 15mH |
| 30V | 1,200μF | 500μF | 250mH | 24mH |
| 25V | 4,000μF | 1,600μF | 400mH | 38mH |
| 20V | 20,000μF | 5,000μF | 1,500mH | 75mH |
| 15V | ** | 25,000μF | ** | 100mH |

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with $I_{LIM}$ = 5A or 20V below the supply rail with $I_{LIM}$ = 2A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

**Secondary breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at $T_C$ = 85°C:

| $\pm V_S$ | SHORT TO $\pm V_S$ C, L, OR EMF LOAD | SHORT TO COMMON |
|---|---|---|
| 50V | .26A | .84A |
| 40V | .38A | 1.1A |
| 35V | .49A | 1.2A |
| 30V | .65A | 1.4A |
| 25V | .84A | 1.7A |
| 20V | 1.1A | 2.2A |
| 15V | 1.4A | 2.9A |

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

# PA12 • PA12A

## POWER OPERATIONAL AMPLIFIERS

## FEATURES

- CURRENT FOLDOVER PROTECTION — NEW
- MIL-STD-883C VERSION — PA12M
- HIGH TEMPERATURE VERSION — PA12H
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±50V
- HIGH OUTPUT CURRENT — up to ±15A Peak

## APPLICATIONS

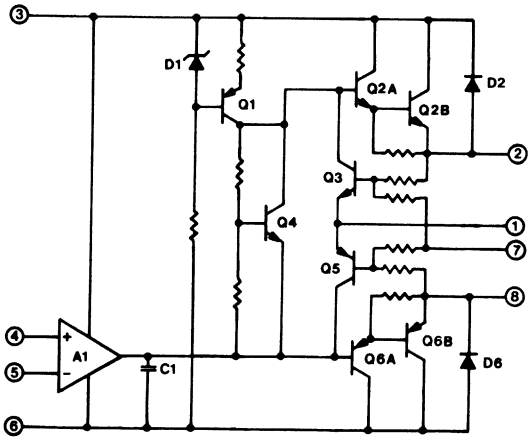
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 10A
- POWER TRANSDUCERS UP TO 100KHz
- TEMPERATURE CONTROL UP TO 360W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 120W RMS

## DESCRIPTION

The PA12 is a state of the art high voltage, very high output current operational amplifier designed to drive resistive, inductive and capacitive loads. The complimentary darlington emitter follower output stage is protected against inductive kickback or back EMF. For optimum linearity especially at low levels, the output state is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. For continuous operation under load, a heatsink of proper rating is recommended. (See AP-Note 1).

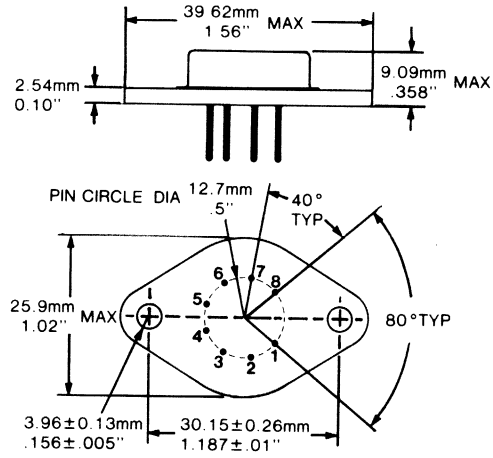
A data sheet supplement for the MIL-STD-883B screened devices is available upon request.

These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is hermetically sealed and isolated. Do no use isolation washers.



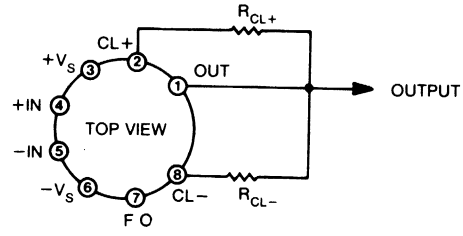



## PACKAGE OUTLINE




| | |
|---|---|
| PIN DIAMETER: | 1.01mm or .04" |
| PIN LENGTH: | 10.2mm or .40" MIN |
| PIN MATERIAL STD: | Nickel plated alloy 52, solderable |
| PIN MATERIAL MIL: | Gold plated alloy 52, solderable |
| PACKAGE: | Hermetic, nickel plated steel |
| ISOLATION: | 300VDC any pin to case |
| SOCKET: | 8 PIN TO-3, APEX PN: MS03 |
| HEATSINKS: | 8 PIN TO-3, APEX PN: HS01 thru HS05 |

## EXTERNAL CONNECTIONS



# PA12 ABSOLUTE MAXIMUM RATINGS

| | PA12 | PA12A |
|---|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 100V | 100V |
| OUTPUT CURRENT, source | 15A | 15A |
| OUTPUT CURRENT, sink | see SOA | see SOA |
| POWER DISSIPATION, internal | 125W | 125W |
| INPUT VOLTAGE, differential | $\pm V_S$ −3V | $\pm V_S$ −3V |
| INPUT VOLTAGE, common-mode | $\pm V_S$ | $\pm V_S$ |
| TEMPERATURE, pin solder-10s | 300°C | 300°C |
| TEMPERATURE, junction[1] | 200°C | 200°C |
| TEMPERATURE RANGE, storage | −65 to +150°C | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −55 to +100°C | −55 to +125°C |

# SPECIFICATIONS

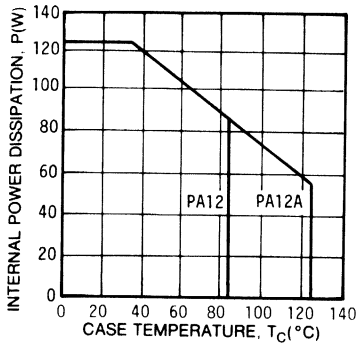
| | | PA12 | | | PA12A | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[2]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C$ = 25°C | | ±2 | ±6 | | ±1 | ±3 | mV |
| OFFSET VOLTAGE, vs. temperature | Full temperature range | | ±10 | ±65 | | * | ±40 | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C$ = 25°C | | ±30 | ±200 | | * | * | µV/V |
| OFFSET VOLTAGE, vs. power | $T_C$ = 25°C | | ±20 | | | * | | µV/W |
| BIAS CURRENT, initial | $T_C$ = 25°C | | 12 | 30 | | 10 | 20 | nA |
| BIAS CURRENT, vs. temperature | Full temperature range | | ±50 | ±400 | | * | * | pA/°C |
| BIAS CURRENT, vs. supply | $T_C$ = 25°C | | ±10 | | | * | | pA/V |
| OFFSET CURRENT, initial | $T_C$ = 25°C | | ±12 | ±30 | | ±5 | ±10 | nA |
| OFFSET CURRENT, vs. temperature | Full temperature range | | ±50 | | | * | | pA/°C |
| INPUT IMPEDANCE, dc | $T_C$ = 25°C | | 200 | | | * | | MΩ |
| INPUT CAPACITANCE | $T_C$ = 25°C | | 3 | | | * | | pF |
| COMMON-MODE VOLTAGE RANGE[3] | Full temperature range | $\pm V_S$ −5 | $\pm V_S$ −3 | | * | * | | V |
| COMMON-MODE REJECTION, dc[3] | Full temp. range, $V_{CM} = \pm V_S$ −6V | 74 | 100 | | * | * | | db |
| **GAIN** | | | | | | | | |
| OPEN LOOP GAIN at 10Hz | $T_C$ = 25°C, 1KΩ load | | 110 | | | * | | db |
| OPEN LOOP GAIN at 10Hz | Full temp. range, 8Ω load | 96 | 108 | | * | * | | db |
| GAIN BANDWIDTH PRODUCT at 1MHz | $T_C$ = 25°C, 8Ω load | | 4 | | | * | | MHz |
| POWER BANDWIDTH | $T_C$ = 25°C, 8Ω load | 13 | 20 | | * | * | | kHz |
| PHASE MARGIN | Full temp. range, 8Ω load | | 20 | | | * | | ° |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[3] | $T_C$=25°C, PA12=10A, PA12A=15A | $\pm V_S$ −6 | | | $\pm V_S$ −7 | | | V |
| VOLTAGE SWING[3] | $T_C$ = 25°C, $I_O$ = 5A | $\pm V_S$ −5 | | | * | | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 80mA | $\pm V_S$ −5 | | | * | | | V |
| CURRENT, peak | $T_C$ = 25°C | 10 | | | 15 | | | A |
| SETTLING TIME to .1% | $T_C$ = 25°C, 2V step | | 2 | | | * | | µs |
| SLEW RATE | $T_C$ = 25°C | 2.5 | 4 | | * | * | | V/µs |
| CAPACITIVE LOAD | Full temp. range, G = 1 | | | 1.5 | | | * | nF |
| CAPACITIVE LOAD | Full temp. range, G > 10 | | | SOA | | | * | |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | Full temperature range | ±10 | ±40 | ±45 | * | * | ±50 | V |
| CURRENT, quiescent | $T_C$ = 25°C | | 25 | 50 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac[4] junction to case | $T_C$ = −55 to +125°C, F>60Hz | | .8 | .9 | | * | * | °C/W |
| RESISTANCE, dc junction to case | $T_C$ = −55 to +125°C | | 1.25 | 1.4 | | * | * | °C/W |
| RESISTANCE, junction to air | $T_C$ = −55 to +125°C | | 30 | | | * | | °C/W |
| TEMPERATURE RANGE, case | Specified as full range | −25 | | +85 | −55 | | +125 | °C |

**NOTES:** * The specification of PA12A is identical to the specification for PA12 in applicable column to the left.

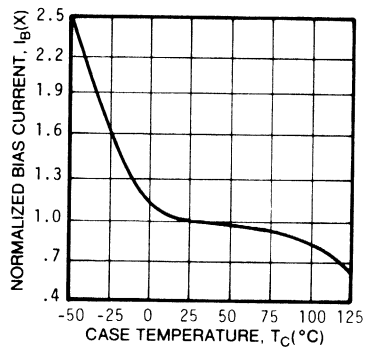
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±40 otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total $V_S$ is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
6. The PA12M is screened to MIL-STD-883C Class B Method 5008. See military models.
7. The PA12H is a low cost high temperature model tested for operation at $T_C$ = 200°C.

# PA12 TYPICAL PERFORMANCE GRAPHS

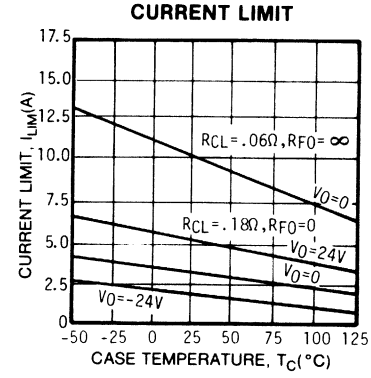
### POWER DERATING



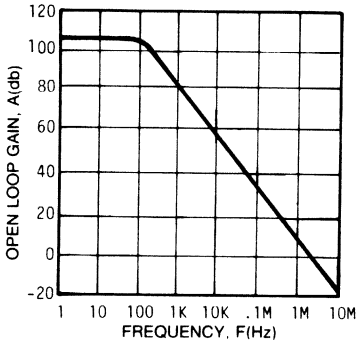

### BIAS CURRENT



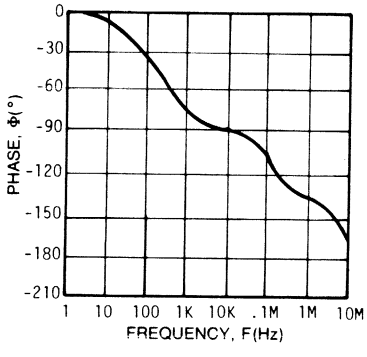

### CURRENT LIMIT



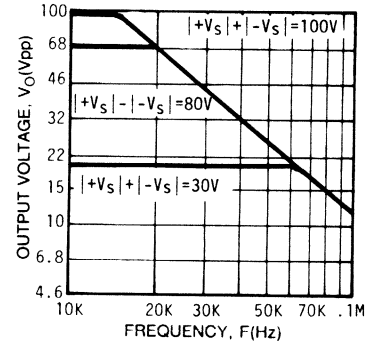

### SMALL SIGNAL RESPONSE



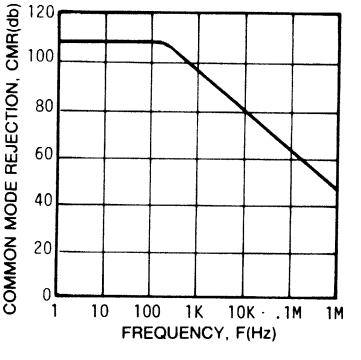

### PHASE RESPONSE



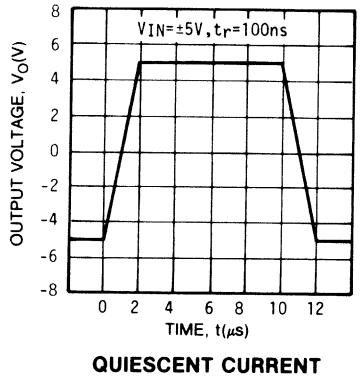

### POWER RESPONSE



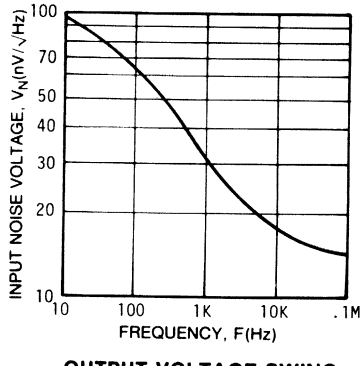

### COMMON MODE REJECTION



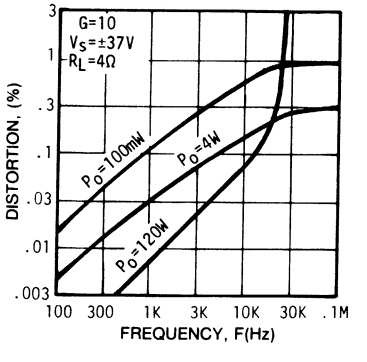

### PULSE RESPONSE



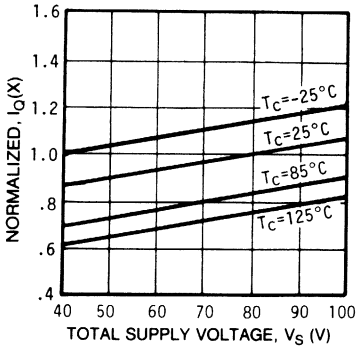

### INPUT NOISE



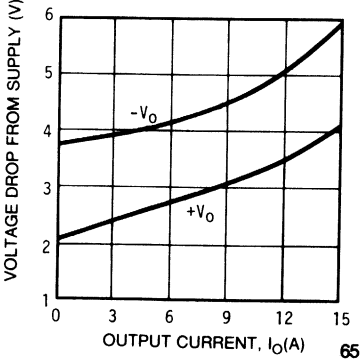

### HARMONIC DISTORTION




### QUIESCENT CURRENT




### OUTPUT VOLTAGE SWING

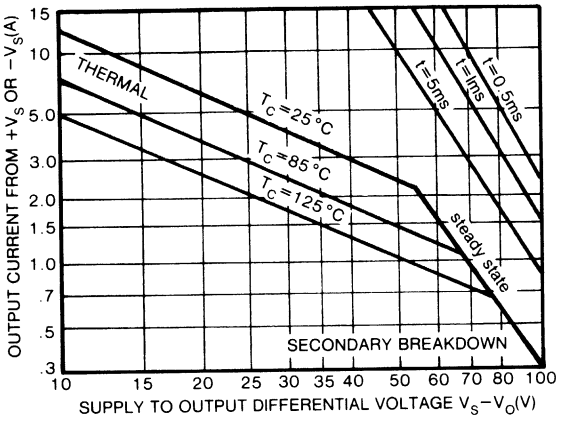


# PA12 OPERATING CONSIDERATIONS

## GENERAL

Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks and mating sockets, see the "Package Outline" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

## SAFE OPERATING AREA (SOA)




The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

1. Capacitive and dynamic* inductive loads up to the following maximums are safe with the current limits set as specified:

| | CAPACITIVE LOAD | | INDUCTIVE LOAD | |
|---|---|---|---|---|
| $\pm V_S$ | $I_{LIM}$ = 5A | $I_{LIM}$ = 10A | $I_{LIM}$ = 5A | $I_{LIM}$ = 10A |
| 50V | 200μF | 125μF | 5mH | 2.0mH |
| 40V | 500μF | 350μF | 15mF | 3.0mH |
| 35V | 2.0mF | 850μF | 50mH | 5.0mH |
| 30V | 7.0mF | 2.5mF | 150mH | 10mH |
| 25V | 25mF | 10mF | 500mH | 20mH |
| 20V | 60mF | 20mF | 1,000mH | 30mH |
| 15V | 150mF | 60mF | 2,500mH | 50mH |

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 10V below the supply rail with Ilim = 15A or 25V below the supply rail with Ilim = 5A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or shorts to common if the current limits are set as follows at $T_C$ = 25C:

| $\pm V_S$ | SHORT TO $\pm V_S$, C, L or EMF LOAD | SHORT TO COMMON |
|---|---|---|
| 50V | .30A | 2.4A |
| 40V | .58A | 2.9A |
| 35V | .87A | 3.7A |
| 30V | 1.5A | 4.1A |
| 25V | 2.4A | 4.9A |
| 20V | 2.9A | 6.3A |
| 15V | 4.2A | 8.0A |

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

## FOLDOVER PROTECTION

For certain applications, foldover protection allows for increased output current as the output of the Power Op Amp swings close to the supply rail. The new version of this Power Op Amp provides such a programmable current foldover protection function. This function can be activated by connecting pin 7 directly or through a resistor to ground, and controlled by the following equation:

$$I_{LIM} = \frac{.65 + \frac{.28\ V_O}{20 + R_{FO}}}{R_{CL} + .007} \quad (1)$$

Where:
$I_{LIM}$ is the current limit at a given output voltage $V_O$.
$R_{FO}$ is the current foldover resistor pin 7 to ground in KΩ.
$R_{CL}$ is the current limit resistors in Ω.
$V_O$ is the instantaneous output voltage in V.

This means that the closer the output swings to the supply rail, the higher the current limit, or inversely; the more voltage is developed across the current carrying output transistors, the lower the current limit.

## PROCEDURE

1. Enter the SOA graph x-axis with the supply voltage and find the maximum short circuit output current on the y-axis.

2. Now calculate the required current limiting resistor for a value of output current below the maximum found on the SOA:

$$R_{CL}(\Omega) = .65/I_{LIM}(A) - .007 \quad (2)$$

3. Find the current limit for the maximum output voltage swing and pin 7 connected to ground/common:

$$I_{LIM} = \frac{.65 + \frac{.28\ V_O}{20}}{R_{CL} + .007} \quad (3)$$

This is the highest current limit possible at maximum output. It may be decreased without effecting the short circuit current limit by putting a resistor in series with pin 7.

The following equation can be used to calculate $R_{FO}$ (KΩ) using a lower current limit:

$$R_{FO} = \frac{.28\ V_O}{I_{CL}(R_{CL} + .007) - .65} - 20 \quad (4)$$

4. To calculate the current limit at any output voltage ($V_O$), use equation "one". If the output transistor has to sink current, assign a negative sign to $V_O$ and check the calculated current against the SOA graph.

5. The power dissipation for $R_C$ is calculated as follows:

$$P(W) = .65\ I_{LIM} \quad (5)$$

6. The power dissipation for $R_{FO}$ should be ¼ W.

## EXAMPLE

1. For Operation with a ±28V Supply at a maximum case temperature of 60°C we interpolate "3A" on the SOA graph.
2. $R_{CL}$ (for 3A) = .22Ω (short circuit protection).
3. Using equation (3) we find $I_{LIM}$ = 4.34A at $V_O$ = 24V and for current sinking $I_{LIM}$ = 1.38A at $V_O$ = −24V.

# PA12H

## POWER OPERATIONAL AMPLIFIERS

## FEATURES

- LOW COST 200°C VERSON OF PA12
- OUTPUT CURRENT at 200°C - ±1A
- FULL SPECIFICATIONS −25 to +125°C
- WIDE SUPPLY RANGE - ±10 to ±45V
- CURRENT FOLDOVER PROTECTION
- EXCELLENT LINEARITY - Class A/B Output

## APPLICATIONS

- MOTOR, VALVE AND ACTUATOR CONTROL
- POWER TRANSDUCERS UP TO 100KHz
- PROGRAMMABLE POWER SUPPLIES UP TO 80V
- TRANSMISSION LINE DRIVER

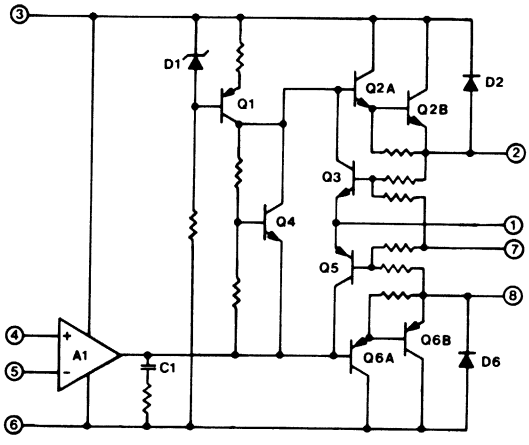
## DESCRIPTION

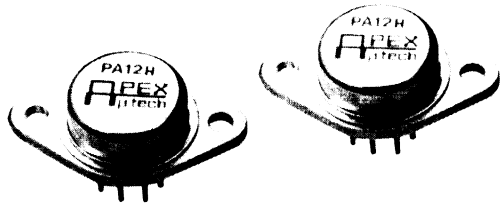
The PA12H is a low cost, high temperature Power Op Amp made especially for short term use in extreme environmental situations such as down hole instrumentation. The amplifier can power mechanical or electronic transducers and can drive the long transmission lines associated with these applications.

The PA12H is based on the standard PA12 because its very high power level leaves a six watt capability after being derated for operation at a case temperature of 200°C. To meet the high temperature requirements for up to 200 hours, polyimid has replaced the standard epoxy for attaching the small signal devices. The melting point of the power transistor attach solder is 264°C.

These hybrid integrated circuits utilize thick film conductors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package (see Package Outlines) is hermetically sealed and isolated. The use of insulating washers is not recommended.

## EQUIVALENT SCHEMATIC




## SPECIFICATIONS

Specifications of the standard PA12 apply to the PA12H with the exception of the temperature range extensions:

1. The operating and storage temperature ranges extend to +200°C.
2. Static and dynamic tests are performed at +125°C as shown in SG 2 and SG 5 of the military PA12M data sheet.
3. Additional tests at $T_C$ = 200°C:
   A. Quiescent current = 100mA max at $\pm V_S$ = 45.
   B. Voltage swing = $\pm V_S$ −4 ($I_O$ = 1A, $\pm V_S$ = 15).

## GENERAL CONSIDERATIONS

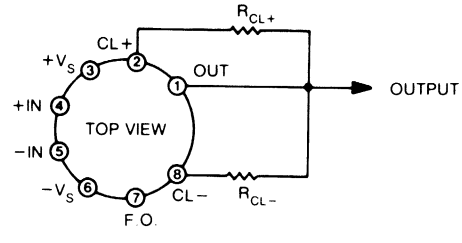
The primary aim of the PA12H is to provide a reasonable level of power output at a minimum cost. To achieve this end, full dynamic tests are performed up to 125°C, with only minimal 100% testing at 200°C. This approach saves nearly an order of magnitude over the cost of a fully tested long life product, but does require recognition of two limitations.

First, input parameters such as voltage offset and bias current are not tested above 125°C. This could lead to accuracy problems if the PA12H is used as a precision computational element. Solutions to this limitation include, contacting the factory regarding additional testing at higher temperatures, or using high temperature small signal amplifiers for computational tasks.

The second limitation of life span requires the PA12H to be used in short term applications. This requirement is mandated by the low cost design concept. At 200°C, component degradation is nearly as severe during storage as during actual operation. This must be taken into account when scheduling actual implementation of the finished package.

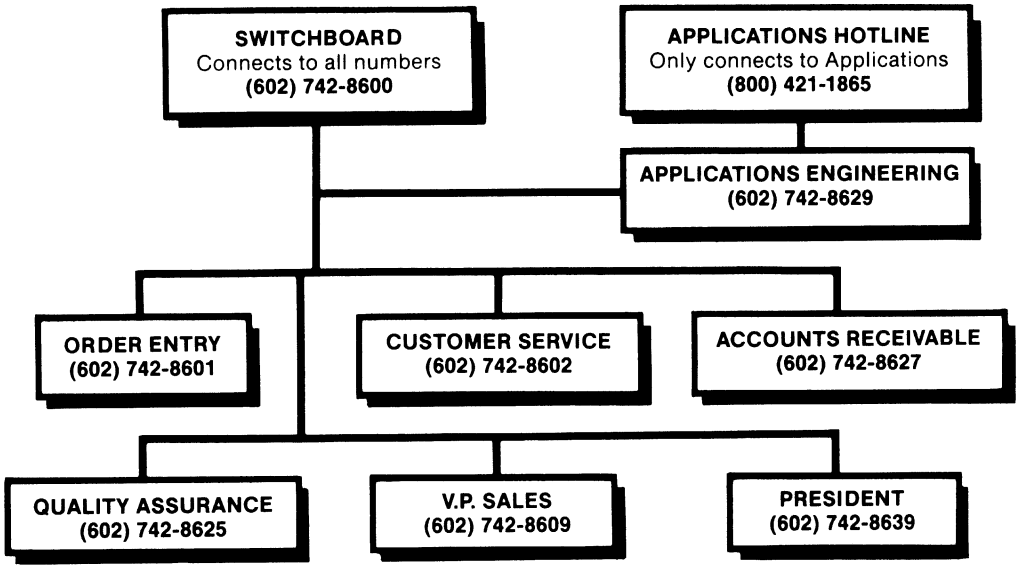
Please consult the PA12 data sheet for basic information on this amplifier, the PA12M data sheet for details on +125°C tests, and Power Operational Amplifier Applications Note 1 "General Operating Considerations," for recommendations on supplies, stability, heatsinks and bypassing.

## EXTERNAL CONNECTIONS



# ACCESS DIRECTORY

## TELEX: 170631




## STANDARD HOURS:

| | MOUNTAIN STANDARD TIME | GREENWICH MEAN TIME |
|---|---|---|
| SWITCH BOARD: | 8:00 AM to 4:30 PM | 15:00 to 23:30 |
| ORDER ENTRY: | 7:00 AM to 5:00 PM | 14:00 to 24:00 |
| OTHER: | 8:00 AM to 4:00 PM | 15:00 to 23:00 |

**APEX MICROTECHNOLOGY CORP. (Domestic)**
**APEX F.S.C. INC. (Export)**
5980 N. SHANNON ROAD, TUCSON, AZ 85741, USA

# PA51 SERIES

## POWER OPERATIONAL AMPLIFIERS

## FEATURES

- WIDE SUPPLY RANGE — ±10 to ±40V
- HIGH OUTPUT CURRENT — ±10A Peak
- SECOND SOURCEABLE — OPA501, 8785
- CLASS "C" OUTPUT — Low Cost
- MIL-STD-883C VERSION — PA51M
- LOW QUIESCENT CURRENT — 2.6mA
- ISOLATED 8 PIN TO-3 CASE — 300 VDC

## APPLICATIONS

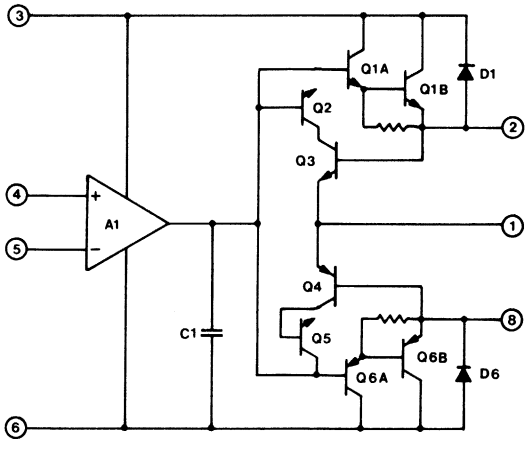
- DC SERVO AMPLIFIER
- MOTOR/SYNCRO DRIVER
- VALVE AND ACTUATOR CONTROL
- DC OR AC POWER REGULATOR

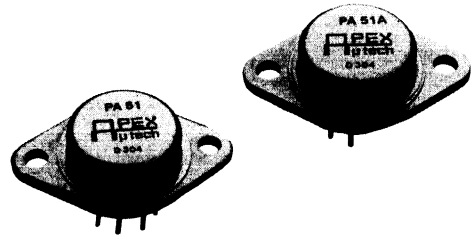
## DESCRIPTION

The PA51 and PA51A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complimentary common emitter output stage is protected against inductive kickback and optimized for low frequency applications where crossover distortion is not critical. These amplifiers are not recommended for audio, transducer or deflection coil drive circuits. The safe operating area (SOA) is fully specified and can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heat sink of proper rating is recommended. Do not use isolation washers!

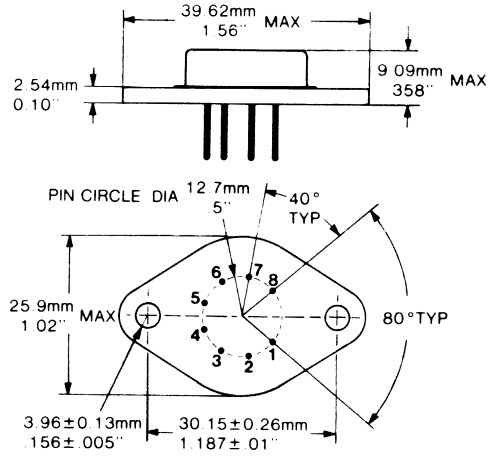
These hybrid integrated circuits utilize thick film conductors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is isolated and hermetically sealed.

## EQUIVALENT SCHEMATIC



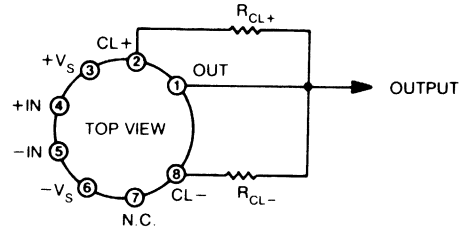




## PACKAGE OUTLINE




| | |
|---|---|
| PIN DIAMETER: | 1.01mm or 0.04" |
| PIN LENGTH: | 10.2mm or 0.40" MIN |
| PIN MATERIAL, STD: | Nickel plated alloy 52, solderable |
| PIN MATERIAL, MIL: | Gold or nickel plated alloy 52, solderable |
| PACKAGE: | Hermetic, nickel plated steel |
| ISOLATION: | 300VDC any pin to case |
| SOCKETS: | APEX PN: MS03 |
| CAGE JACKS: | APEX PN: MS02 (set of 8) |
| HEATSINKS: | APEX PNs: HS01 thru HS05 |

## EXTERNAL CONNECTIONS



# PA51 SERIES ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 80V |
| OUTPUT CURRENT, source | 10A |
| OUTPUT CURRENT, sink | see SOA |
| POWER DISSIPATION, internal | 97W |
| INPUT VOLTAGE, differential | $\pm V_S$ −3V |
| INPUT VOLTAGE, common-mode | $\pm V_S$ |
| TEMPERATURE, junction[1] | 200°C |
| TEMPERATURE, pin solder-10s | 300°C |
| TEMPERATURE RANGE, storage | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −55 to +125°C |

# SPECIFICATIONS

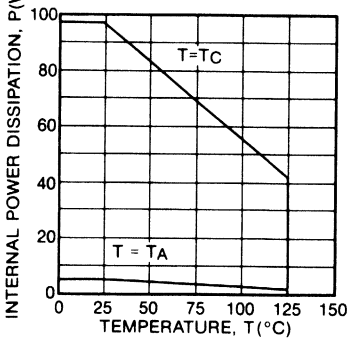
| | | PA51/PA51B | | | PA51A/PA51C | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[2]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C$ = 25°C | | ±5 | ±10 | | ±2 | ±5 | mV |
| OFFSET VOLTAGE, vs. temperature | Full temperature range | | ±10 | ±65 | | * | ±40 | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C$ = 25°C | | ±35 | | | * | | µV/V |
| OFFSET VOLTAGE, vs. power | $T_C$ = 25°C | | ±20 | | | * | | µV/W |
| BIAS CURRENT, initial | $T_C$ = 25°C | | ±15 | ±40 | | * | ±20 | nA |
| BIAS CURRENT, vs. temperature | Full temperature range | | ±.05 | | | * | | nA/°C |
| BIAS CURRENT, vs. supply | $T_C$ = 25°C | | ±.02 | | | * | | nA/V |
| OFFSET CURRENT, initial | $T_C$ = 25°C | | ±5 | ±10 | | ±2 | ±3 | nA |
| OFFSET CURRENT, vs. temperature | Full temperature range | | ±.01 | | | * | | nA/°C |
| INPUT IMPEDANCE, common-mode | $T_C$ = 25°C | | 250 | | | * | | MΩ |
| INPUT IMPEDANCE, differential | $T_C$ = 25°C | | 10 | | | * | | MΩ |
| INPUT CAPACITANCE | $T_C$ = 25°C | | 3 | | | * | | pF |
| COMMON-MODE VOLTAGE RANGE[3] | Full temperature range | $\pm V_S$ −6 | $\pm V_S$ −3 | | * | * | | V |
| COMMON-MODE REJECTION, dc[3] | $T_C$ = 25°C, $V_{CM} = \pm V_S$ −6V | 70 | 110 | | 80 | * | | db |
| **GAIN** | | | | | | | | |
| OPEN LOOP GAIN at 10Hz | Full temp. range, full load | 94 | 115 | | 98 | * | | db |
| GAIN BANDWIDTH PRODUCT at 1MHz | $T_C$ = 25°C, full load | | 1 | | * | * | | MHz |
| POWER BANDWIDTH | $T_C$ = 25°C, $I_O$ = 8A, $V_O = 40V_{PP}$ | 10 | 16 | | | * | | kHz |
| PHASE MARGIN | Full temperature range | | 45 | | | * | | ° |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[3] | $T_C$ = 25°C, $I_O$ = 10A | $\pm V_S$ −8 | $\pm V_S$ −5 | | * | * | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 4A | $\pm V_S$ −6 | $\pm V_S$ −4 | | * | | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 68mA | $\pm V_S$ −6 | | | * | | | V |
| CURRENT | $T_C$ = 25°C | ±10 | | | * | | | A |
| SETTLING TIME to .1% | $T_C$ = 25°C, 2V step | | 2 | | | * | | µs |
| SLEW RATE | $T_C$ = 25°C, $R_L$ = 6Ω | ±1.0 | 2.6 | | * | * | | V/µs |
| CAPACITIVE LOAD, unit gain | Full temperature range | | | 1.5 | | | * | nF |
| CAPACITIVE LOAD, gain>4 | Full temperature range | | | SOA | | | * | |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | Full temperature range | ±10 | ±28 | ±36 | * | ±34 | ±40 | V |
| CURRENT, quiescent | $T_C$ = 25°C | | 2.6 | 10 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac junction to case[4] | F>60Hz | | 1.0 | 1.2 | | * | * | °C/W |
| RESISTANCE, dc junction to case | F<60Hz | | 1.5 | 1.8 | | * | * | °C/W |
| RESISTANCE, junction to air | | | 30 | | | * | | °C/W |
| TEMPERATURE RANGE, case | Meet full range specification | −25/ −55 | 25 | +85/ +125 | −55/ −25 | * | +125/ +85 | °C |

**NOTES:** * The specification of PA51A/PA51C is identical to the specification for PA51/PA51B in applicable column to the left.

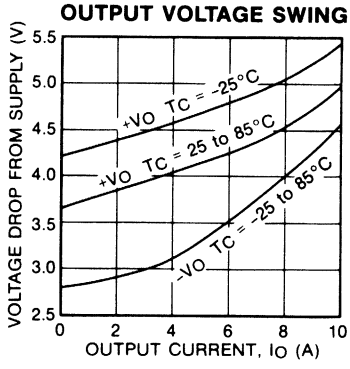
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total $V_S$ is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
6. The PA51M is screened to MIL-STD-883C Class B Method 5008. See military models.

# PA51 SERIES TYPICAL PERFORMANCE GRAPHS

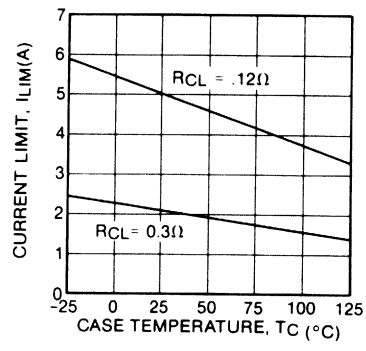
### POWER DERATING



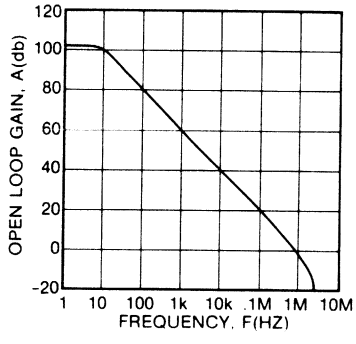

### OUTPUT VOLTAGE SWING



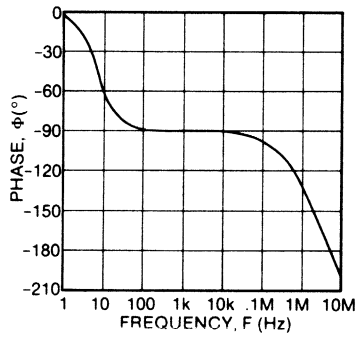

### CURRENT LIMIT



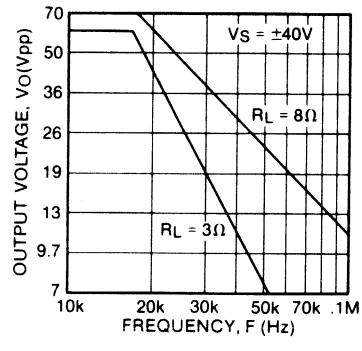

### SMALL SIGNAL RESPONSE



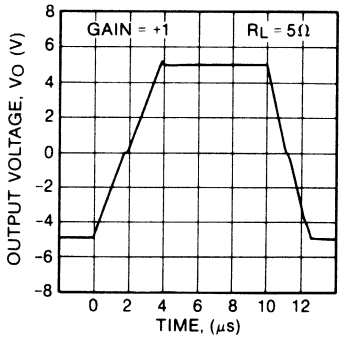

### PHASE RESPONSE



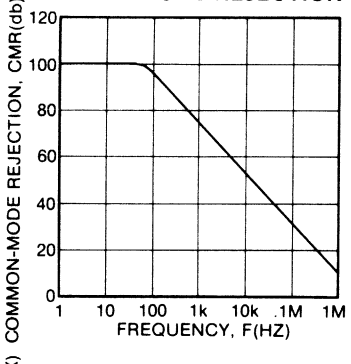

### POWER RESPONSE



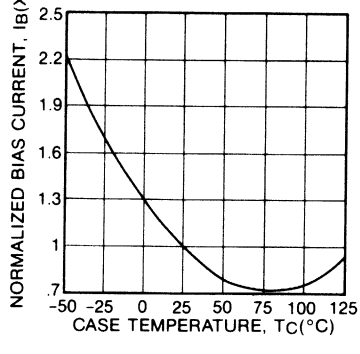

### PULSE RESPONSE



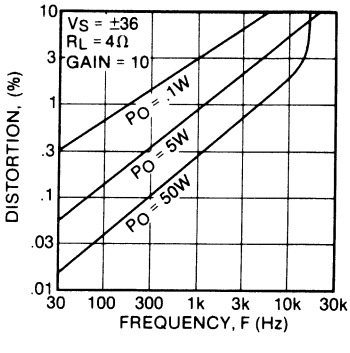

### COMMON-MODE REJECTION



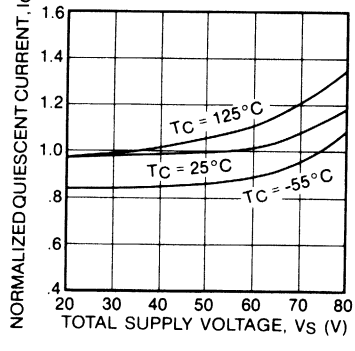

### BIAS CURRENT



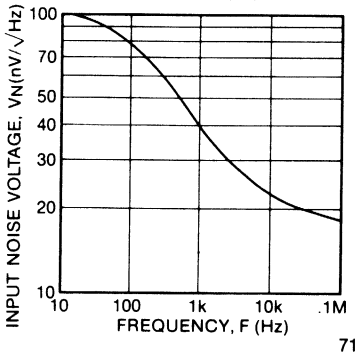

### HARMONIC DISTORTION




### QUIESCENT CURRENT




### INPUT NOISE



# PA51 OPERATING CONSIDERATIONS

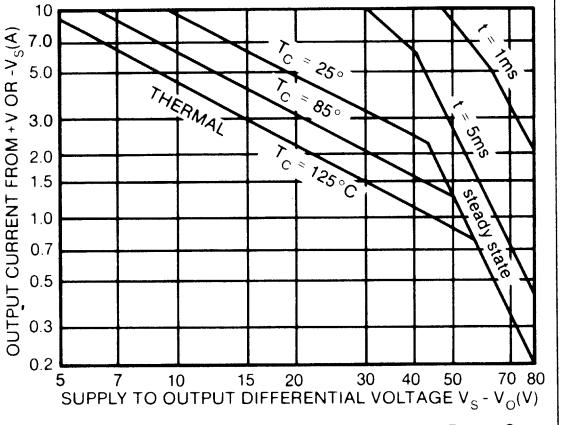
## GENERAL

Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks and mating sockets, see the "Package Outline" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

## SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The secondary breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.




The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximums are safe:

| | CAPACITIVE LOAD | | INDUCTIVE LOAD | |
|---|---|---|---|---|
| ±V$_S$ | I$_{LIM}$ = 5A | I$_{LIM}$ = 10A | I$_{LIM}$ = 5A | I$_{LIM}$ = 10A |
| 40V | 400µF | 200µF | 11mH | 4.3mH |
| 35V | 800µF | 400µF | 20mH | 5.0mH |
| 30V | 1600µF | 800µF | 35mH | 6.2mH |
| 25V | 5.0mF | 2.5mF | 50mH | 15mH |
| 20V | 10mF | 5.0mF | 400mH | 20mH |
| 15V | 20mF | 10mF | ** | 100mH |

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I$_{LIM}$ = 10A or 15V below the supply rail with I$_{LIM}$ = 5A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

**Secondary breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or shorts to common if the current limits are set as follows at T$_C$ = 85° C.

| ±V$_S$ | SHORT TO ±V$_S$, C, L OR EMF LOAD | SHORT TO COMMON |
|---|---|---|
| 40V | 0.2A | 1.5A |
| 35V | 0.3A | 1.6A |
| 30V | 0.5A | 2.0A |
| 25V | 1.2A | 2.4A |
| 20V | 1.5A | 3.0A |
| 15V | 2.0A | 4.0A |

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

# PA61 • PA61A

## POWER OPERATIONAL AMPLIFIER

## FEATURES

- WIDE SUPPLY RANGE - ±10 to ±45V
- HIGH OUTPUT CURRENT - ±10A Peak
- LOW COST - Class "C" output stage
- MIL-STD-883C VERSION - PA61M
- LOW QUIESCENT CURRENT - 3mA
- ISOLATED 8 PIN TO-3 CASE - 300VDC

## APPLICATIONS

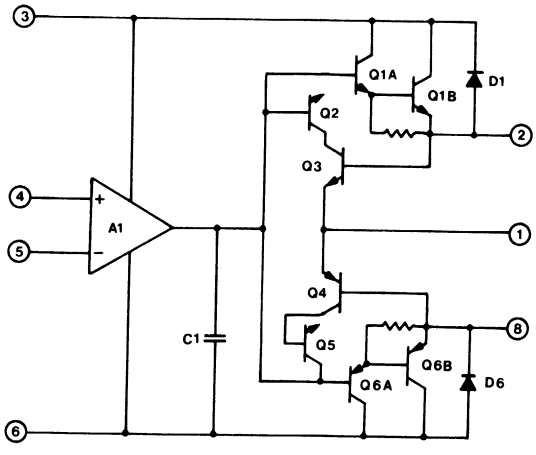
- PROGRAMMABLE POWER SUPPLY
- MOTOR/SYNCRO DRIVER
- VALVE AND ACTUATOR CONTROL
- DC OR AC POWER REGULATOR
- FIXED FREQUENCY POWER OSCILLATOR

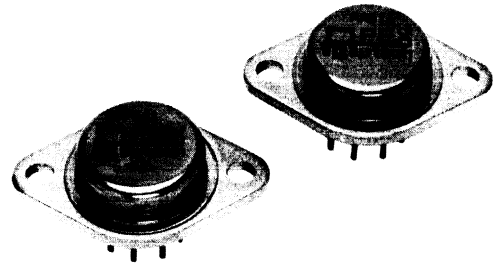
## DESCRIPTION

The PA61 and PA61A are high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complimentary emitter follower output stage is protected against inductive kickback and optimized for low frequency applications where crossover distortion is not critical. These amplifiers are not recommended for audio, transducer or deflection coil drive circuits above 1kHz or when distortion is critical. The safe operating area (SOA) is fully specified and can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended. Do not use isolation washers!

These hybrid integrated circuits utilize thick film conductors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is isolated and hermetically sealed.

## EQUIVALENT SCHEMATIC



## TYPICAL APPLICATIONS

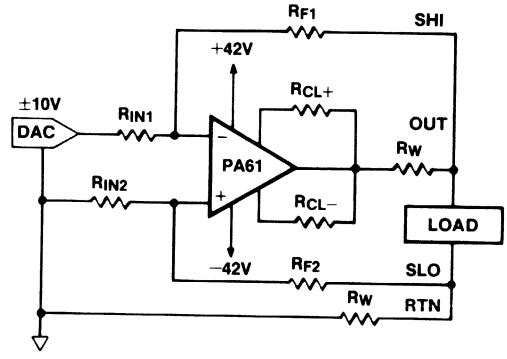
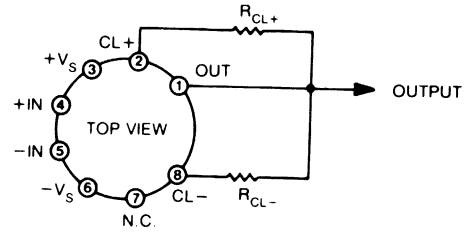



**FIGURE 1. Programmable Power Supply with Remote Sensing.**

Due to its high current drive capability, PA61 applications often utilize remote sensing to compensate IR drops in the wiring. The importance of remote sensing increases as accuracy requirements, output currents and distance between amplifier and load go up. The circuit above shows wire resistance from the PA61 to the load and back to the local ground via the power return line. Without remote sensing, a 7.5A load current across only 0.05 ohm in each line would produce a 0.75V error at the load.

With the addition of the second ratio matched $R_F/R_{IN}$ pair and two low current sense wires, IR drops in the power return line become common mode voltages for which the op amp has a very high rejection ratio. Voltage drops in the output and power return wires are inside the feedback loop. Therefore, as long as the Power Op Amp has the voltage drive capability to overcome the IR losses, accuracy remains the same. Application Note 7 presents a general discussion of PPS circuits.

## EXTERNAL CONNECTIONS



# PA61 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 90V |
| OUTPUT CURRENT, source | 10A |
| OUTPUT CURRENT, sink | see SOA |
| POWER DISSIPATION, internal | 97W |
| INPUT VOLTAGE, differential | $\pm V_S$ −3V |
| INPUT VOLTAGE, common-mode | $\pm V_S$ |
| TEMPERATURE, junction[1] | 200°C |
| TEMPERATURE, pin solder-10s | 300°C |
| TEMPERATURE RANGE, storage | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −55 to +125°C |

# SPECIFICATIONS

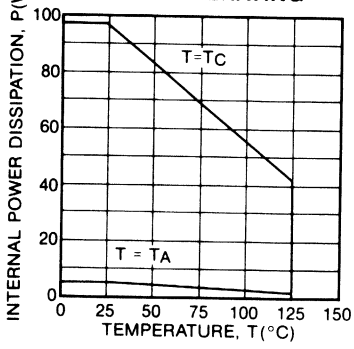
| | | PA61 | | | PA61A | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[2]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C$ = 25°C | | ±2 | ±6 | | ±1 | ±3 | mV |
| OFFSET VOLTAGE, vs. temperature | Specified temperature range | | ±10 | ±65 | | * | ±40 | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C$ = 25°C | | ±30 | ±200 | | * | * | µV/V |
| OFFSET VOLTAGE, vs. power | $T_C$ = 25°C | | ±20 | | | * | | µV/W |
| BIAS CURRENT, initial | $T_C$ = 25°C | | 12 | 30 | | 10 | 20 | nA |
| BIAS CURRENT, vs. temperature | Specified temperature range | | ±50 | ±400 | | * | * | pA/°C |
| BIAS CURRENT, vs. supply | $T_C$ = 25°C | | ±10 | | | * | | pA/V |
| OFFSET CURRENT, initial | $T_C$ = 25°C | | ±12 | ±30 | | ±5 | ±10 | nA |
| OFFSET CURRENT, vs. temperature | Specified temperature range | | ±50 | | | * | | pA/°C |
| INPUT IMPEDANCE, dc | $T_C$ = 25°C | | 200 | | | * | | MΩ |
| INPUT CAPACITANCE | $T_C$ = 25°C | | 3 | | | * | | pF |
| COMMON-MODE VOLTAGE RANGE[3] | Specified temperature range | $\pm V_S$ −5 | $\pm V_S$ −3 | | * | * | | V |
| COMMON-MODE REJECTION, dc[3] | Specified temperature range | 74 | 100 | | * | * | | db |
| **GAIN** | | | | | | | | |
| OPEN LOOP GAIN at 10Hz | Full temp. range, full load | 96 | 108 | | * | * | | db |
| GAIN BANDWIDTH PRODUCT at 1MHz | $T_C$ = 25°C, full load | | 1 | | | * | | MHz |
| POWER BANDWIDTH | $T_C$ = 25°C, $I_O$ = 8A, $V_O$ = 40$V_{PP}$ | 10 | 16 | | * | * | | kHz |
| PHASE MARGIN | Full temperature range | | 45 | | | * | | ° |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[3] | $T_C$ = 25°C, $I_O$ = 10A | $\pm V_S$ −7 | $\pm V_S$ −5 | | $\pm V_S$ −6 | * | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 4A | $\pm V_S$ −6 | $\pm V_S$ −4 | | * | * | | V |
| VOLTAGE SWING[3] | Full temp. range, $I_O$ = 68mA | $\pm V_S$ −5 | | | * | | | V |
| CURRENT | $T_C$ = 25°C | ±10 | | | | * | | A |
| SETTLING TIME to .1% | $T_C$ = 25°C, 2V step | | 2 | | * | * | | µs |
| SLEW RATE | $T_C$ = 25°C, $R_L$ = 6Ω | 1.0 | 2.8 | | | | * | V/µs |
| CAPACITIVE LOAD, unit gain | Full temperature range | | | 1.5 | | | * | nF |
| CAPACITIVE LOAD, gain>4 | Full temperature range | | | SOA | | | | |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | Full temperature range | ±10 | ±32 | ±45 | * | * | * | V |
| CURRENT, quiescent | $T_C$ = 25°C | | 3 | 10 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac junction to case[4] | F>60Hz | | 1.0 | 1.2 | | * | * | °C/W |
| RESISTANCE, dc junction to case | F<60Hz | | 1.5 | 1.8 | | * | * | °C/W |
| RESISTANCE, junction to air | | | 30 | | | * | | °C/W |
| TEMPERATURE RANGE, case | Meet full range specification | −25 | 25 | +85 | * | * | * | °C |

**NOTES:** * The specification of PA61A is identical to the specification for PA61 in applicable column to the left.

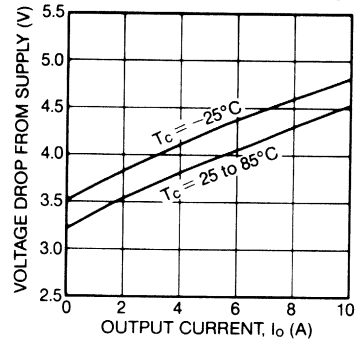
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total $V_S$ is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
6. The PA61M is screened to MIL-STD-883C Class B Method 5008. See Military Models.

# PA61 TYPICAL PERFORMANCE GRAPHS

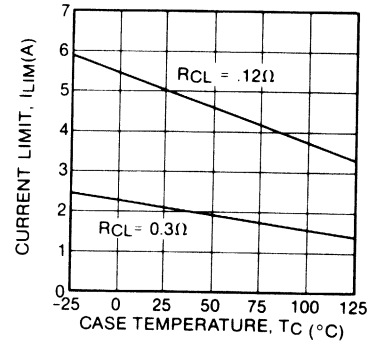
### POWER DERATING



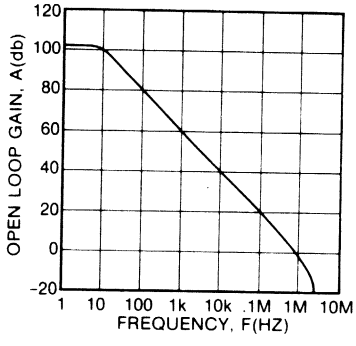

### OUTPUT VOLTAGE SWING



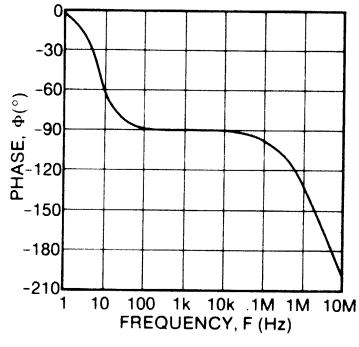

### CURRENT LIMIT



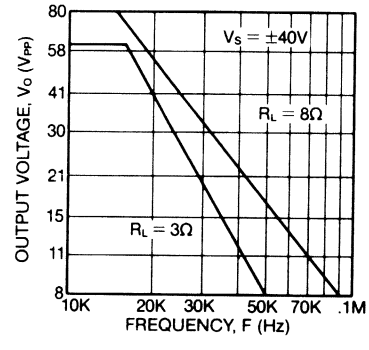

### SMALL SIGNAL RESPONSE



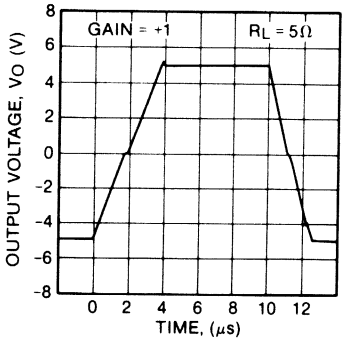

### PHASE RESPONSE



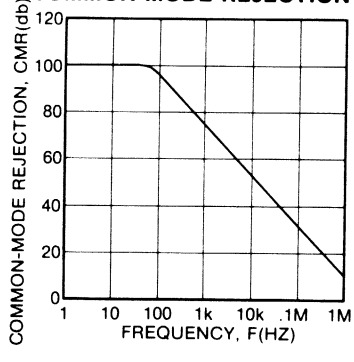

### POWER RESPONSE



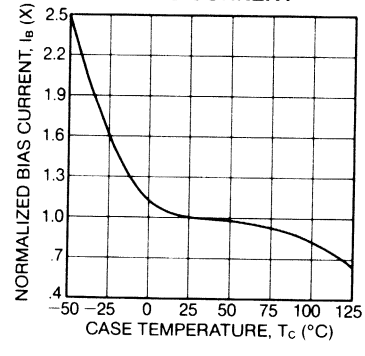

### PULSE RESPONSE



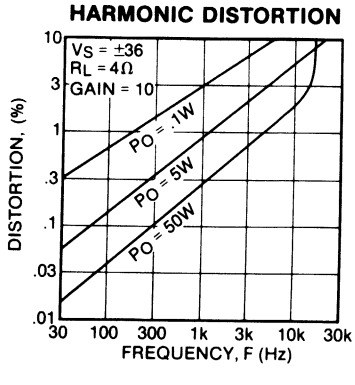

### COMMON-MODE REJECTION



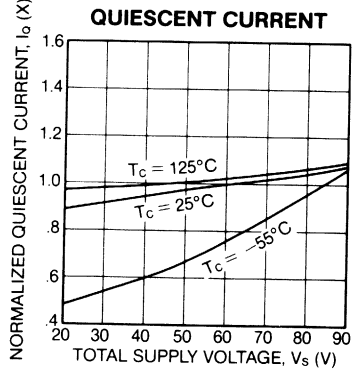

### BIAS CURRENT



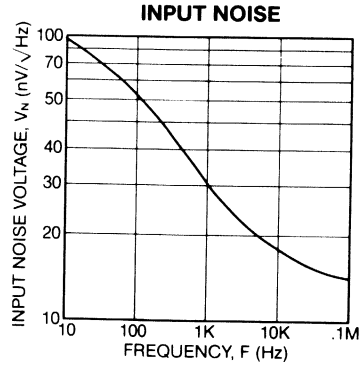

### HARMONIC DISTORTION




### QUIESCENT CURRENT




### INPUT NOISE



# PA61 OPERATING CONSIDERATIONS

## GENERAL

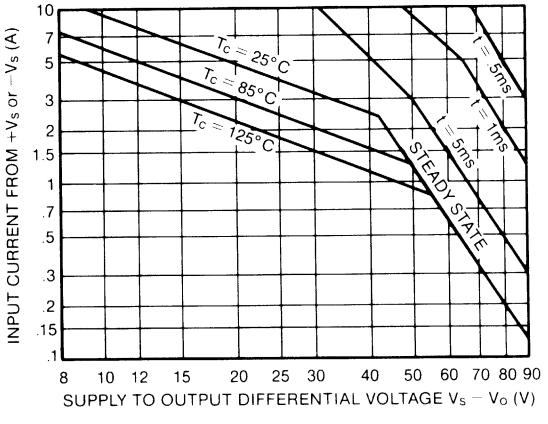
Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks, and mating sockets, see the "Package Outlines" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

## SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The secondary breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.

## PA61 SAFE OPERATING AREA (SOA)




The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximum are safe:

| | CAPACITIVE LOAD | | INDUCTIVE LOAD | |
|---|---|---|---|---|
| $\pm V_S$ | $I_{LIM}$ = 5A | $I_{LIM}$ = 10A | $I_{LIM}$ = 5A | $I_{LIM}$ = 10A |
| 45V | 200μF | 150μF | 8mH | 2.8mH |
| 40V | 400μF | 200μF | 11mH | 4.3mH |
| 35V | 800μF | 400μF | 20mH | 5.0mH |
| 30V | 1600μF | 800μF | 35mH | 6.2mH |
| 25V | 5.0mF | 2.5mF | 50mH | 15mH |
| 20V | 10mF | 5.0mF | 400mH | 20mH |
| 15V | 20mF | 10mF | ** | 100mH |

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with $I_{LIM}$ = 10A or 15V below the supply rail with $I_{LIM}$ = 5A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

**Secondary breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at $T_C$ = 85°C.

| $\pm V_S$ | SHORT TO $\pm V_S$ C, L, OR EMF LOAD | SHORT TO COMMON |
|---|---|---|
| 45V | 0.1A | 1.3A |
| 40V | 0.2A | 1.5A |
| 35V | 0.3A | 1.6A |
| 30V | 0.5A | 2.0A |
| 25V | 1.2A | 2.4A |
| 20V | 1.5A | 3.0A |
| 15V | 2.0A | 4.0A |

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

# PA80 SERIES
## POWER OPERATIONAL AMPLIFIERS

## FEATURES

- HIGH VOLTAGE OPERATION - ±150V (PA82J)
- HIGH OUTPUT CURRENT - ±60mA (PA80J)
- PROTECTED OUTPUT - Thermal Shutoff
- LOW BIAS CURRENT, LOW NOISE - FET Input
- SECOND SOURCEABLE - BB3580J, 81J, 82J

## APPLICATIONS

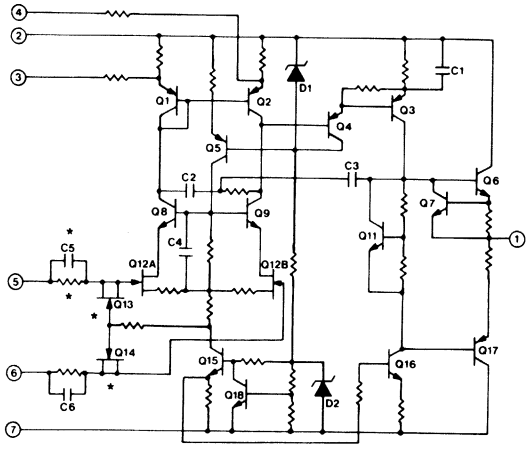
- HIGH IMPEDANCE BUFFERS UP TO ±140V
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES TO ±145V
- BIOCHEMISTRY STIMULATORS
- COMPUTER TO VACUUM TUBE INTERFACE

## DESCRIPTION

The PA80 series of high voltage operation amplifiers provides an extremely wide range of supply capability with three overlapping products. High accuracy is achieved with a cascade input circuit configuration. All internal biasing is referenced to a zener diode. As a result these models offer outstanding common mode and power supply rejection. The output stage operates in the class A/B mode for best linearity. Internal phase compensation assures stability at all gain settings without external components. Fixed internal current limits protect these amplifiers against a short circuit to common at most supply voltages. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A built-in thermal shutoff circuit prevents destructive overheating under most abnormal operating conditions. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

These hybrid integrated circuits utilize thick film conductors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. Insulating washers are not recommended.

## EQUIVALENT SCHEMATIC




* NOTE: Not used for PA80S


## TYPICAL APPLICATIONS

### High Voltage Programmable Power Supply

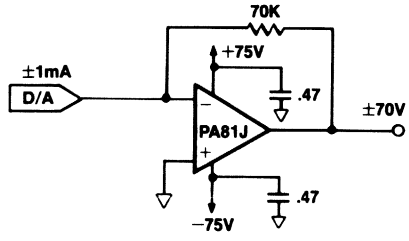
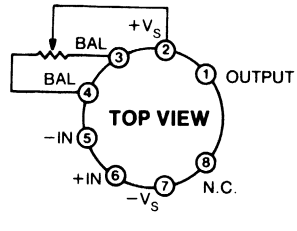



**FIGURE 1. HIGH VOLTAGE PROGRAMMABLE POWER SUPPLY.**

The PA81 and 70 ohm resistor form a current to voltage converter, accepting ±1mA from a 12 bit current output digital to analog converter. The power op amp contribution to the error budget is insignificant. At a case temperature of 70°C, the combination of voltage offset and bias errors amounts to less than 31 ppm of full scale range. Incorporation of the optional offset trim can further reduce these errors to under 9 ppm.

## EXTERNAL CONNECTIONS




NOTES:
1. Input offset trimpot optional. Recommended value 100KΩ.

# PA80 SERIES ABSOLUTE MAXIMUM RATINGS

| | PA80J | PA81J | PA82J |
|---|---|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 70V | 150V | 300V |
| OUTPUT CURRENT, source | | Internally Limited | |
| POWER DISSIPATION, internal | | 11.5W | |
| INPUT VOLTAGE, differential | ±50V | ±150V | ±300V |
| INPUT VOLTAGE, common mode | | $\pm V_S$ | |
| TEMPERATURE, pin solder-10sec | | 300°C | |
| TEMPERATURE, storage | | −65 to 125°C | |
| TEMPERATURE RANGE, powered (case) | | −55 to 125°C | |

# SPECIFICATIONS

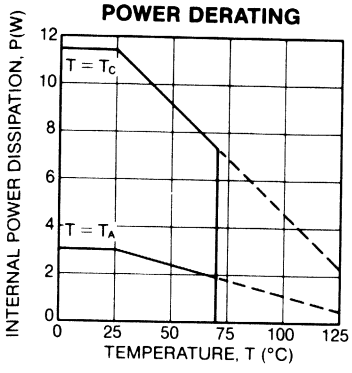
| | | PA80J | | | PA81J | | | PA82J | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST COND.** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | | | | |
| Offset Voltage, initial | $T_C = 25°C$ | | ±5 | ±10 | | ±1.5 | ±3 | | ±1.5 | ±3 | mV |
| vs. temp. | Full temp. range | | 10 | 30 | | 10 | 25 | | 10 | 25 | µV/°C |
| vs. supply | $T_C = 25°C$ | | 100 | | | 20 | | | * | | µV/V |
| vs. time | $T_C = 25°C$ | | 150 | | | 75 | | | * | | µV√kh |
| Bias Current, initial | $T_C = 25°C$ | | 5 | 50 | | * | * | | * | * | pA |
| vs. supply | $T_C = 25°C$ | | .5 | | | .2 | | | * | | pA/V |
| Offset Current, initial | $T_C = 25°C$ | | 2.5 | 50 | | * | * | | * | * | pA |
| Input Impedance, dc | $T_C = 25°C$ | | $10^{11}$ | | | * | | | * | * | Ω |
| Input Capacitance | $T_C = 25°C$ | | 10 | | | * | | | * | * | pF |
| Common Mode | | | | | | | | | | | |
| Voltage Range[2] | Full temp. range | $\pm V_S - 10$ | | | * | | | * | | | V |
| Rejection, dc | $V_{CM} = \pm 20V$ | | 86 | | | 110 | | * | * | | db |
| **GAIN** | | | | | | | | | | | |
| Open Loop at 10Hz | Full load | 86 | 104 | | 94 | 116 | | 100 | 118 | | db |
| Unity Gain Bandwidth | $T_C = 25°C$ | | 5 | | | * | | | * | | MHz |
| Power Bandwidth | $T_C = 25°C$, full load | | 100 | | | 60 | | | 30 | | kHz |
| Phase Margin | Full temp. range | | 45 | | | * | | | * | | ° |
| **OUTPUT** | | | | | | | | | | | |
| Voltage Swing[2] | $T_C = 25°C$, $I_{PK}$ | $\pm V_S - 5$ | | | * | | | * | | | V |
| Current, peak | $T_C = 25°C$ | 60 | | | 30 | | | 15 | | | mA |
| Current, limit | $T_C = 25°C$ | | 100 | | | 50 | | | 25 | | mA |
| Settling Time to .1% | $T_C = 25°C$, 10V step | | 12 | | | * | | | * | | µs |
| Slew Rate | $T_C = 25°C$ | | 15 | | | 20 | | | * | | V/µs |
| Capacitive Load | G = 1 | | 10 | | | * | | | * | | nF |
| **POWER SUPPLY** | | | | | | | | | | | |
| Voltage | Full temp. range | ±15 | ±35 | ±35 | ±32 | ±75 | ±75 | ±70 | ±150 | ±150 | V |
| Current, quiescent | $T_C = 25°C$ | | 8.5 | 10 | * | 6.5 | 8.5 | | 6.5 | 8.5 | mA |
| **THERMAL** | | | | | | | | | | | |
| Resistance, | | | | | | * | | | * | | |
| ac[3], junction to case | F>60Hz | | 6 | | | | | | | | °C/W |
| Resistance, | | | | | | * | * | | * | * | |
| dc, junction to case | F<60Hz | | 9 | 10 | | * | | | * | | °C/W |
| Resistance, case to air | Full temp. range | | 30 | | | * | | | * | | °C/W |
| Temp., shutdown | | | 150 | | | | * | * | | * | °C |
| Temp. Range, case | Full range spec. | 0 | | 70 | * | | | | | | °C |

**NOTES:** * The specification is identical to the specification for the model in applicable column to the left.

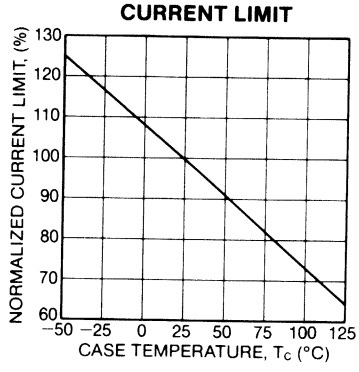
1. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
2. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total $V_S$ is measured from $+V_S$ to $-V_S$.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
4. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
5. On the PA81J and PA82J, signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.

# PA80 SERIES TYPICAL PERFORMANCE CURVES

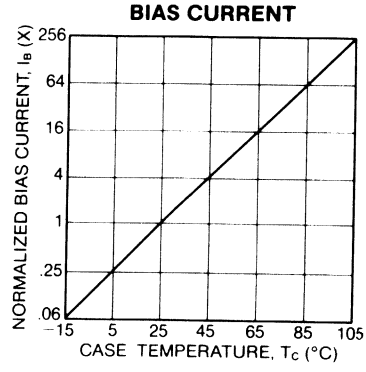
## POWER DERATING



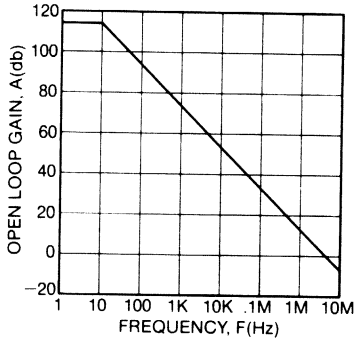

## CURRENT LIMIT



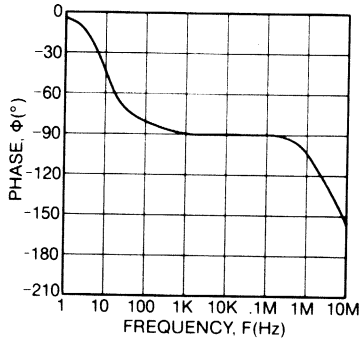

## BIAS CURRENT



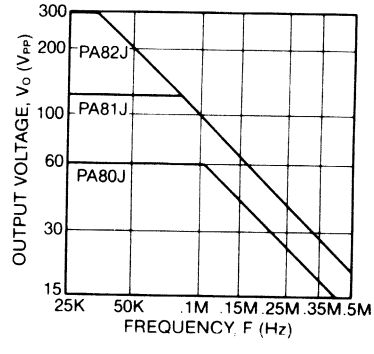

## SMALL SIGNAL RESPONSE



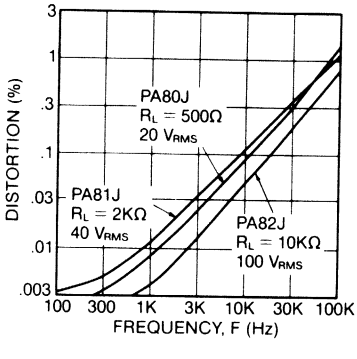

## PHASE RESPONSE



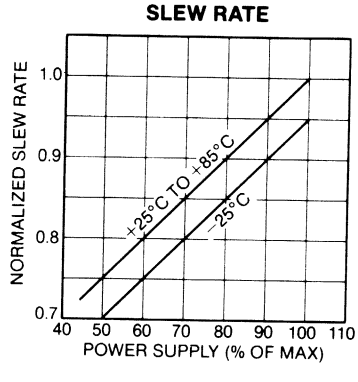

## POWER RESPONSE



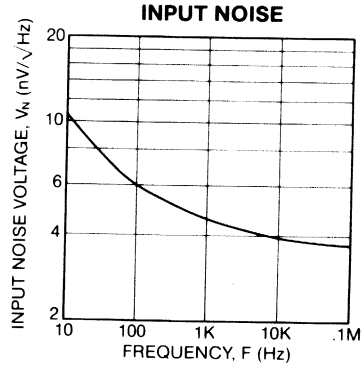

## HARMONIC DISTORTION



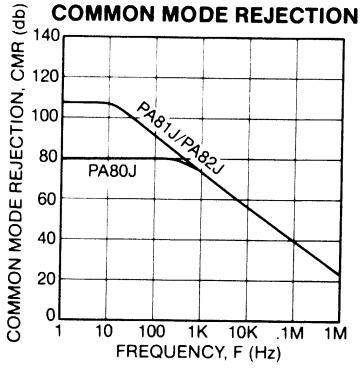

## SLEW RATE



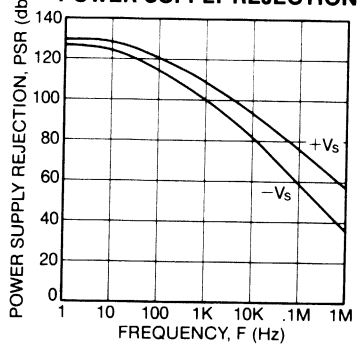

## INPUT NOISE



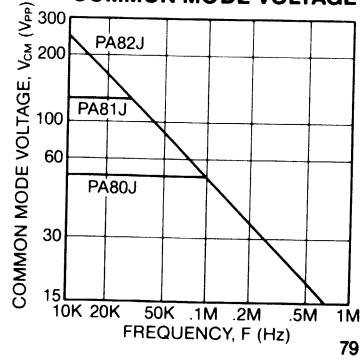

## COMMON MODE REJECTION




## POWER SUPPLY REJECTION




## COMMON MODE VOLTAGE



# PA80 SERIES OPERATING CONSIDERATIONS

## GENERAL

Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, interpretation of specifications, and symbols used. The information given here cover specific considerations for the PA80J, 81J and 82J. For information on the package outline, heatsinks, and mating sockets, see the "Package Outlines" and "Accessories" sections of the APEX Power Op Amp Handbook.

## SAFE OPERATING AREA (SOA)

For PA80J and PA81J, the combination of voltage capability and internal current limits mandate that the devices are safe for all combinations of supply voltage and load. On the PA82J, any load combination is safe up to a total supply of 250 volts. When total supply voltage equals 300 volts, the device will be safe if the output current is limited to 10 milliamps or less. This means that the PA82J used on supplies up to ±125 volts will sustain a short to common or either supply without danger. When using supplies above ±125 volts, a short to one of the supplies will be potentially destructive. When using single supply above 250 volts, a short to common will be potentially destructive.

Safe supply voltages do not imply disregard for heatsinking. The thermal calculations and the use of a heatsink are required in many applications to maintain the case temperature within the specified operating range of 0 to 70°C. Exceeding this case temperature range can result in an inoperative circuit due to excessive input errors or activation of the thermal shutdown.

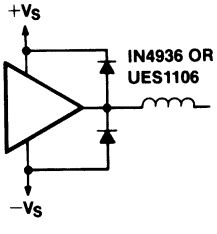



**FIGURE 2. PROTECTION, INDUCTIVE LOAD**

## INDUCTIVE LOADS

Two external diodes as shown in figure 2, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltage of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

## THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds safe limits. This allows the heatsink design to be based solely on normal conditions but prevents excessive temperatures during abnormal high power conditions without overdesigning the heatsink.

Under abnormal operating conditions, activation of the thermal shutdown is a sign that the internal temperatures have reached approximately 150°. Continued operation in this temperature range will reduce the life of the product. Also, in this operating mode the device may oscillate in and out of thermal shutoff destroying useful signals.

## SINGLE SUPPLY OPERATION

These amplifiers are suitable for operation from a single supply voltage. The operating requirements do however, impose the limitation that the input voltages do not approach closer than 10 volts to either supply rail. Referring to the simplified schematics, this is due to the operating voltage requirements of the current sources, the half-dynamic loads and the cascade stage. Thus, single supply operation requires the input signals to be biased at least 10 volts from either supply rail. Figure 3 illustrates one bias technique to achieve this.

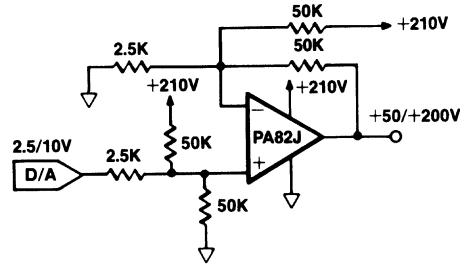



**FIGURE 3. TRUE SINGLE SUPPLY OPERATION.**

Figure 4 illustrates a very common deviation from true single supply operation. The availability of two supplies still allows ground (common) referenced signals but also maximizes the high voltage capability of the unipolar output. This technique can utilize an existing low voltage system power supply and does not place large current demands on that supply. The 12 volt supply in this case must supply only the quiescent current of the PA81J, which is 8.5mA maximum. If the load is reactive or EMF producing, the low voltage supply must also be able to absorb the reverse currents generated by the load.

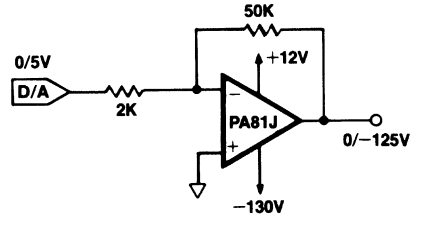



**FIGURE 4. NON-SYMMETRIC SUPPLIES.**

# PA83 • PA83A

## POWER OPERATIONAL AMPLIFIERS

## FEATURES

- MIL-STD-883C VERSION — PA83M
- LOW BIAS CURRENT, LOW NOISE — FET Input
- PROTECTED OUTPUT — Thermal Shutoff
- FULLY PROTECTED INPUT — Up to ±150V
- WIDE SUPPLY RANGE — ±15V to ±150V
- SECOND SOURCEABLE — BB3583AM/JM

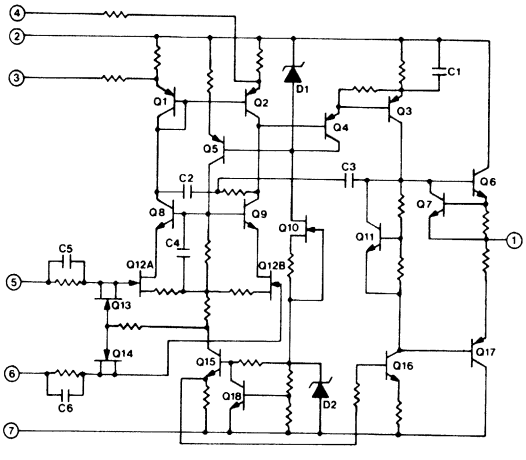
## APPLICATIONS

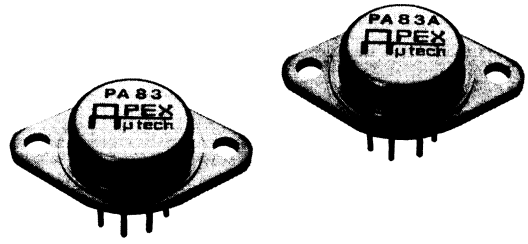
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 290V
- ANALOG SIMULATORS

## DESCRIPTION

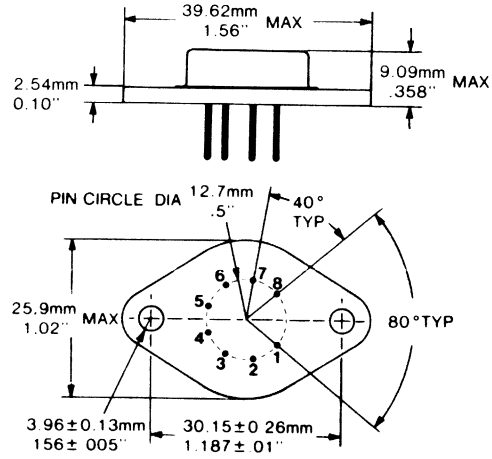
The PA83 is a high voltage operational amplifier designed for output voltage swings of up to ±145V with a dual (±) supply or 290V with a single supply. Its input stage is protected against transient and steady state overvoltages up to and including the supply rails. High accuracy is achieved with a cascade input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA83 features an unprecedented supply range and excellent supply rejection. The output stage is biased in the class A/B mode for linear operation. Internal phase compensation assures stability at all gain settings without need for external components. Fixed current limits protect these amplifiers against shorts to common at supply voltages up to 120V. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A built-in thermal shutoff circuit prevents destructive overheating. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

These hybrid integrated circuits utilize beryllia (BeO) substrates, thick (cermet) film resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is hermetically sealed by resistance welding.



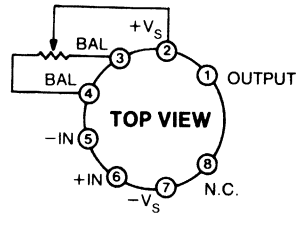




## PACKAGE OUTLINE




| | |
|---|---|
| PIN DIAMETER: | 1.01mm or 0.04" |
| PIN LENGTH: | 10.2mm or 0.40" MIN |
| PIN MATERIAL, STD: | Nickel plated alloy 52, solderable |
| PIN MATERIAL, MIL: | Gold or nickel plated alloy 52, solderable |
| PACKAGE: | Hermetic, nickel plated steel |
| ISOLATION: | 300VDC any pin to case |
| SOCKETS: | APEX PN: MS03 |
| CAGE JACKS: | APEX PN: MS02 (set of 8) |
| HEATSINKS: | APEX PNs: HS01 thru HS05 |

## EXTERNAL CONNECTIONS




NOTES: 1. Pin 8 not internally connected.
2. Input offset trimpot optional. Recommended value 100KΩ.

# PA83 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 300V |
| OUTPUT CURRENT, source | Internally Limited |
| OUTPUT CURRENT, sink | see SOA |
| POWER DISSIPATION, internal at $T_C = 85°C$[1] | 17.5W |
| INPUT VOLTAGE, differential | ±300V |
| INPUT VOLTAGE, common-mode | ±300V |
| TEMPERATURE, pin solder-10s max (solder) | 300°C |
| TEMPERATURE RANGE, storage | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −55 to +125°C |

# SPECIFICATIONS

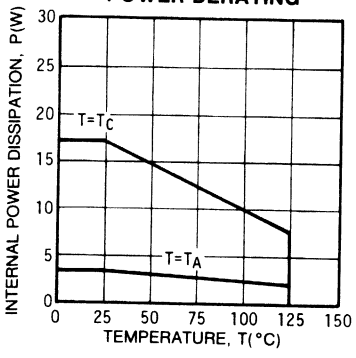
| | | PA83 | | | PA83A | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS**[2] | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C = 25°C$ | | ±1.5 | ±3 | | ±.5 | ±1 | mV |
| OFFSET VOLTAGE, vs. temperature | Full temperature range | | ±10 | ±25 | | ±5 | ±10 | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C = 25°C$ | | ±.5 | | | ±.2 | | µV/V |
| OFFSET VOLTAGE, vs. time | $T_C = 25°C$ | | ±75 | | | * | | µV/√kh |
| BIAS CURRENT, initial[3] | $T_C = 25°C$ | | 5 | 50 | | 3 | 10 | pA |
| BIAS CURRENT, vs. supply | $T_C = 25°C$ | | .01 | | | * | | pA/V |
| OFFSET CURRENT, initial[3] | $T_C = 25°C$ | | ±2.5 | ±50 | | ±1.5 | ±10 | pA |
| OFFSET CURRENT, vs. supply | $T_C = 25°C$ | | ±.01 | | | * | | pA/V |
| INPUT IMPEDANCE, dc | $T_C = 25°C$ | | $10^{11}$ | | | * | | Ω |
| INPUT CAPACITANCE | Full temperature range | | 6 | | | * | | pF |
| COMMON-MODE VOLTAGE RANGE[4] | Full temperature range | $\pm V_S - 10$ | | | * | | | V |
| COMMON-MODE REJECTION, dc | Full temperature range | | 130 | | | * | | db |
| **GAIN** | | | | | | | | |
| OPEN LOOP GAIN at 10Hz | $T_C = 25°C$, $R_L = 2K\Omega$ | 96 | 116 | | * | * | | db |
| UNITY GAIN CROSSOVER FREQ. | $T_C = 25°C$, $R_L = 2K\Omega$ | | 5 | | 3 | * | | MHz |
| POWER BANDWIDTH | $T_C = 25°C$, $R_L = 10K\Omega$ | | 60 | | 40 | * | | kHz |
| PHASE MARGIN | Full temperature range | | 60 | | | * | | ° |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[4], full load | Full temp. range, $I_O = 75mA$ | $\pm V_S - 10$ | $\pm V_S - 5$ | | * | * | | V |
| VOLTAGE SWING[4] | Full temp. range, $I_O = 15mA$ | $\pm V_S - 5$ | $\pm V_S - 3$ | | * | * | | V |
| CURRENT, peak | $T_C = 25°C$ | 75 | | | * | | | mA |
| CURRENT, short circuit | $T_C = 25°C$ | | 100 | | | * | | mA |
| SLEW RATE | $T_C = 25°C$, $R_L = 2K\Omega$ | 20 | 30 | | * | * | * | V/µs |
| CAPACITIVE LOAD, unity gain | Full temperature range | | | 10 | | | * | nF |
| CAPACITIVE LOAD, gain>4 | Full temperature range | | | SOA | | | * | µF |
| SETTLING TIME to 0.1% | $T_C = 25°C$, $R_L = 2K\Omega$, 10V step | | 12 | | | * | | µs |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | $T_C = -55$ to $+125°C$ | ±15 | ±150 | ±150 | * | * | * | V |
| CURRENT, quiescent | $T_C = 25°C$ | | 6 | 8.5 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac[5] junction to case | F>60Hz | | 3.8 | | | * | | °C/W |
| RESISTANCE, dc junction to case | F<60Hz | | 6 | 6.5 | | * | * | °C/W |
| RESISTANCE, case to air | | | 30 | | | * | | °C/W |
| TEMPERATURE RANGE, case | Meet full range specification | −25 | | +85 | * | | * | °C |

**NOTES:** * The specification of PA83A is identical to the specification for PA83 in applicable column to the left.

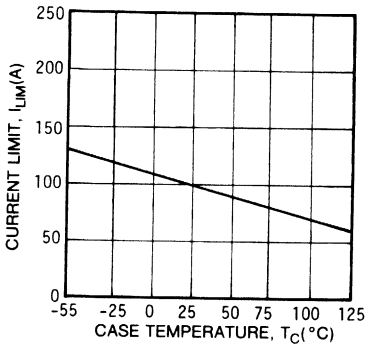
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is the TYP rating unless otherwise specified as a test condition.
3. Doubles for every 10°C of temperature increase
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
7. The PA83M is screened to MIL-STD-883C Class B Method 5008. See military models.
8. Signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.

# PA83 TYPICAL PERFORMANCE GRAPHS

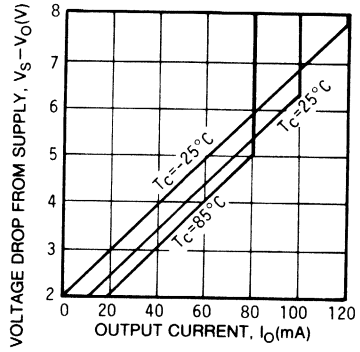
### POWER DERATING



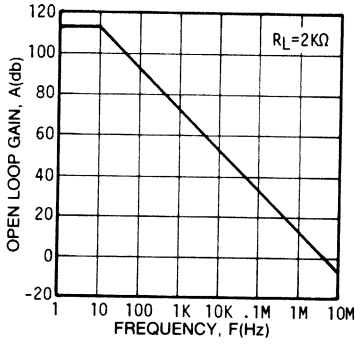

### CURRENT LIMIT



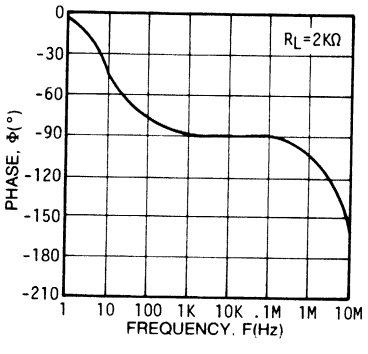

### OUTPUT VOLTAGE SWING



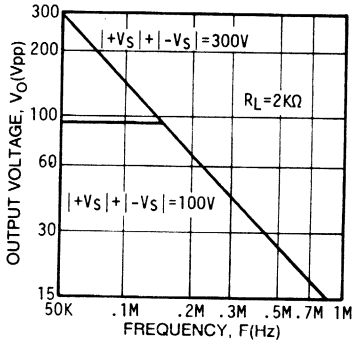

### SMALL SIGNAL RESPONSE



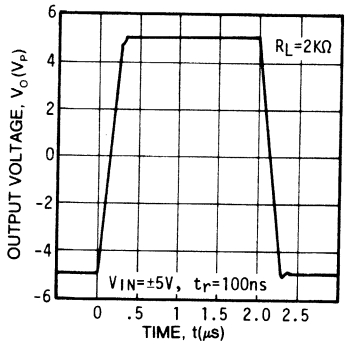

### PHASE RESPONSE



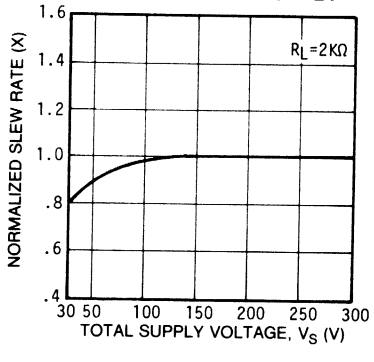

### POWER RESPONSE



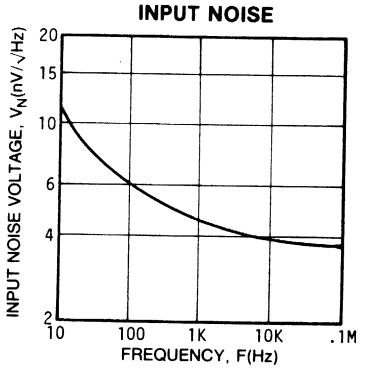

### PULSE RESPONSE



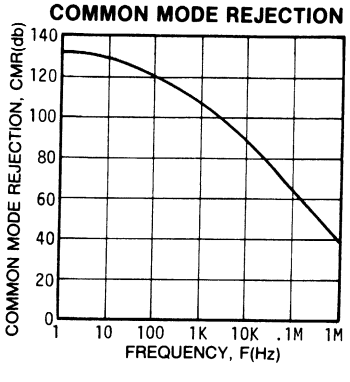

### SLEW RATE VS. SUPPLY



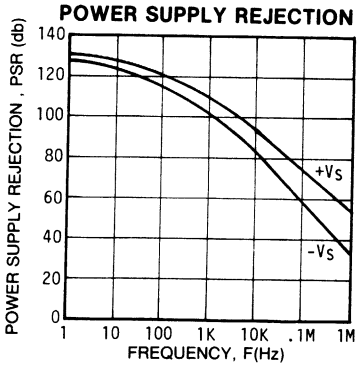

### INPUT NOISE



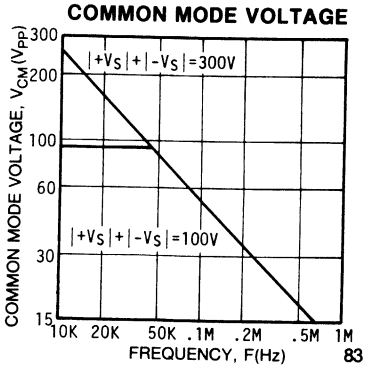

### COMMON MODE REJECTION




### POWER SUPPLY REJECTION




### COMMON MODE VOLTAGE



# PA83 OPERATING CONSIDERATIONS

## GENERAL

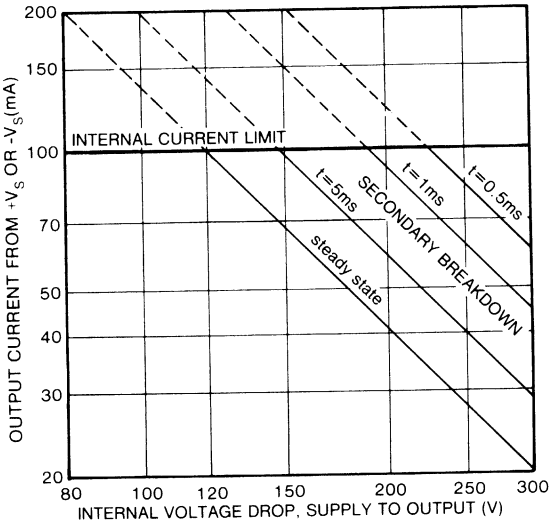
Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks and mating sockets, see the "Package Outline" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

## SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The secondary breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.

## SAFE OPERATING AREA CURVES




The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. The following capacitive and inductive loads are safe:

| $\pm V_S$ | C(MAX) | L(MAX) |
|---|---|---|
| 150V | .7μF | 1.5H |
| 125V | 2.0μF | 2.5H |
| 100V | 5.0μF | 6.0H |
| 75V | 60μF | 30H |
| 50V | ALL | ALL |

2. Short circuits to ground are safe with dual supplies up to ±120V or single supplies up to 120V.
3. Short circuits to the supply rails are safe with total supply voltages up to 120V. (ie ±60V).

## THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds safe limits. This allows the heatsink design to be based solely on normal conditions but prevents excessive temperatures during abnormal high power conditions without overdesigning the heatsink.

Under abnormal operating conditions, activation of the thermal shutdown is a sign that the internal temperatures have reached approximately 150°. Continued operation in this temperature range will reduce the life of the product. Also, in this operating mode the device may oscillate in and out of thermal shutoff destroying useful signals.

## INDUCTIVE LOADS

Two external diodes as shown in figure 1, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

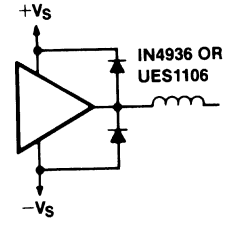



**FIGURE 1. PROTECTIVE, INDUCTIVE LOAD.**

# PA84 • PA84A • PA84S

## POWER OPERATIONAL AMPLIFIERS

## FEATURES

- HIGH SLEW RATE — 200V/μs
- FAST SETTLING TIME — .1% in 1μs (PA84S)
- FULLY PROTECTED INPUT — Up to ±150V
- LOW BIAS CURRENT, LOW NOISE — FET Input
- WIDE SUPPLY RANGE — ±15V to ±150V
- MIL-STD-883C VERSION — PA84M
- SECOND SOURCEABLE — BB3584JM

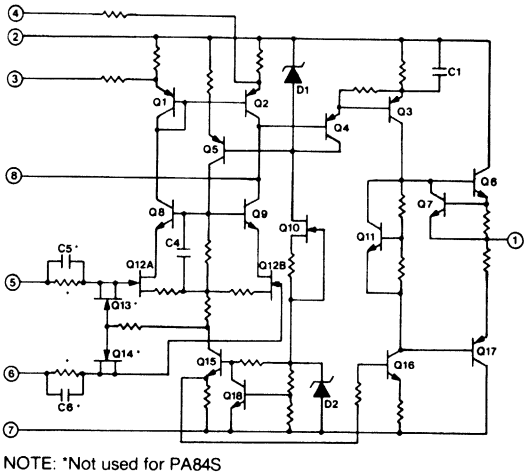
## APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 290V
- ANALOG SIMULATORS

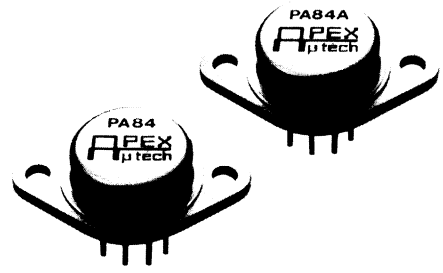
## DESCRIPTION

The PA84 is a high voltage operational amplifier designed for output voltage swings up to ±145V with a dual (±) supply or 290V with a single supply. Two versions are available. The new PA84S, fast settling amplifier can absorb differential input overvoltages up to ±50V while the established PA84 and PA84A can handle input overvoltages of up to ±300V. Both versions are protected against common-mode transients and overvoltages up to the supply rails. High accuracy is achieved with a cascade input configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA84 features an unprecedented supply range and excellent supply rejection. The output stage is biased-on for linear operation. External phase compensation allows for user flexibility in obtaining the maximum slew rate. Fixed current limits protect these amplifiers against shorts to common at supply voltages up to 150V. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A built-in thermal shutoff circuit prevents destructive overheating. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

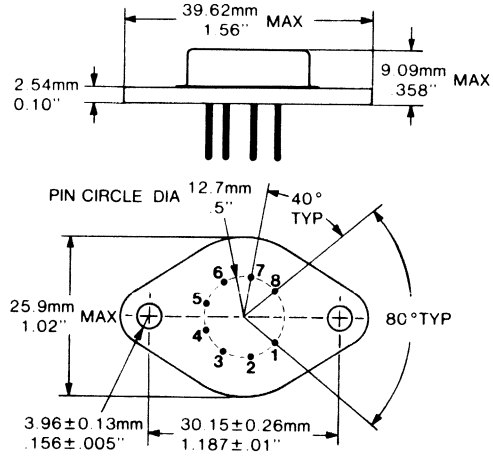
These hybrid integrated circuits utilize beryllia (BeO) substrates, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is hermetically sealed by resistance welding.




NOTE: *Not used for PA84S

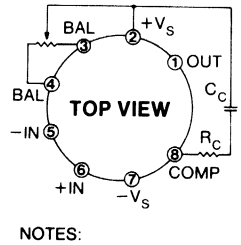



## PACKAGE OUTLINE




| | |
|---|---|
| PIN DIAMETER: | 1.01mm or .04" |
| PIN LENGTH: | 10.2mm or .40" MIN |
| PIN MATERIAL STD: | Nickel plated alloy 52, solderable |
| PIN MATERIAL MIL: | Gold plated alloy 52, solderable |
| PACKAGE: | Hermetic, nickel plated steel |
| ISOLATION: | 300VDC any pin to case |
| SOCKET: | APEX PN: MS03 |
| CAGE JACKS: | APEX PN: MS02 (set of 8) |
| HEATSINKS: | APEX PN: HS01-HS05 |

## EXTERNAL CONNECTIONS




### PHASE COMPENSATION

| GAIN | Cc | Rc |
|---|---|---|
| 1 | 10nf | 200Ω |
| 10 | 500pf | 2KΩ |
| 100 | 50pf | 20KΩ |
| 1000 | not required | not required |

NOTES:
1. Phase Compensation required for safe operation.
2. Input offset trimpot optional. Recommended value 100KΩ.

# PA84 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 300V |
| OUTPUT CURRENT, source | INTERNALLY LIMITED |
| OUTPUT CURRENT, sink | see SOA |
| POWER DISSIPATION, internal at $T_C = 85°C$ | 17.5W |
| INPUT VOLTAGE, differential PA84/PA84A[1] | ±300V |
| INPUT VOLTAGE, differential PA84S | ±50V |
| INPUT VOLTAGE, common-mode[1] | $\pm V_S$ |
| TEMPERATURE, pins for 10s max (solder) | 300°C |
| TEMPERATURE, junction[2] | 200°C |
| TEMPERATURE RANGE, storage | −65 to +150°C |
| TEMPERATURE RANGE, powered (case) | −55 to +125°C |

# SPECIFICATIONS

| | | PA84/PA84S | | | PA84A | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[3]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | $T_C = 25°C$ | | ±1.5 | ±3 | | ±.5 | ±1 | mV |
| OFFSET VOLTAGE, vs. temperature | $T_C = -25$ to $+85°C$ | | ±10 | ±25 | | ±5 | ±10 | µV/°C |
| OFFSET VOLTAGE, vs. supply | $T_C = 25°C$ | | ±.5 | | | ±.2 | | µV/V |
| OFFSET VOLTAGE, vs. time | $T_C = 25°C$ | | ±75 | | | * | | $\mu V/\sqrt{kh}$ |
| BIAS CURRENT, initial[4] | $T_C = 25°C$ | | 5 | 50 | | 3 | 10 | pA |
| BIAS CURRENT, vs. supply | $T_C = 25°C$ | | .01 | | | * | | pA/V |
| OFFSET CURRENT, initial[4] | $T_C = 25°C$ | | ±2.5 | ±50 | | ±1.5 | ±10 | pA |
| OFFSET CURRENT, vs. supply | $T_C = 25°C$ | | ±.01 | | | * | | pA/V |
| INPUT IMPEDANCE, dc | $T_C = 25°C$ | | $10^{11}$ | | | * | | Ω |
| INPUT CAPACITANCE | $T_C = -25$ to $+85°C$ | | 6 | | | * | | pF |
| COMMON-MODE VOLTAGE RANGE[5] | $T_C = -25$ to $+85°C$ | $\pm V_S - 10$ | $\pm V_S - 8.5$ | | * | * | | V |
| COMMON-MODE REJECTION, dc | $T_C = -25$ to $+85°C$ | | 130 | | | * | | db |
| **GAIN** | | | | | | | | |
| OPEN LOOP at 10Hz | $T_C = 25°C$, $R_L = \infty$ | | 120 | | | * | | db |
| OPEN LOOP at 10Hz | $T_C = 25°C$, $R_L = 3.5K\Omega$ | 100 | 118 | | * | * | | db |
| GAIN BANDWIDTH PRODUCT at 1MHz | $T_C = 25°C$, $R_L = 3.5K\Omega$, $R_C = 20K\Omega$ | | 75 | | | * | | MHz |
| POWER BANDWIDTH, high gain | $T_C = 25°C$, $R_L = 3.5K\Omega$, $R_C = 20K\Omega$ | | 250 | | 180 | * | | KHz |
| POWER BANDWIDTH, low gain | $T_C = 25°C$, $R_L = 3.5K\Omega$, $R_C = 2K\Omega$ | | 120 | | | * | | KHz |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING[5] | $T_C = 25°C$, $I_O = \pm 40mA$ | $\pm V_S - 7$ | $\pm V_S - 3$ | | * | * | | V |
| VOLTAGE SWING[5] | $T_C = -25$ to $+85°C$, $I_O = \pm 15mA$ | $\pm V_S - 5$ | $\pm V_S - 2$ | | * | * | | V |
| CURRENT, peak | $T_C = 25°C$ | 40 | | | * | | | mA |
| CURRENT, short circuit | $T_C = 25°C$ | | 50 | | | * | | mA |
| SLEW RATE, high gain | $T_C = 25°C$, $R_L = 3.5K\Omega$, $R_C = 20K\Omega$ | | 200 | | 150 | * | | V/µs |
| SLEW RATE, low gain | $T_C = 25°C$, $R_L = 3.5K\Omega$, $R_C = 2K\Omega$ | | 125 | | | * | | V/µs |
| SETTLING TIME, .01% at gain = 100 | $T_C = 25°C$, $R_L = 3.5K\Omega$ | | 20/2 | | | 20 | | µs |
| SETTLING TIME, .1% at gain = 100 | $R_C = 20K\Omega$, $V_{IN} = 2V$ step | | 12/1 | | | 12 | | µs |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | $T_C = -55$ to $+125°C$ | ±15 | | ±150 | * | | * | V |
| CURRENT, quiescent | $T_C = 25°C$ | | 5.5 | 7.5 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, ac[6] junction to case | $T_C = -55$ to $+125°C$ | | 3.8 | | | * | | °C/W |
| RESISTANCE, dc junction to case | $T_C = -55$ to $+125°C$ | | 6 | 6.5 | | * | * | °C/W |
| RESISTANCE, case to air | $T_C = -55$ to $+125°C$ | | 30 | | | * | | °C/W |

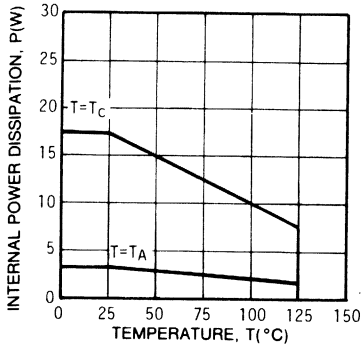
**NOTES:**

*The specification of PA84A is identical to the specification for PA84/PA84S in applicable column to left.

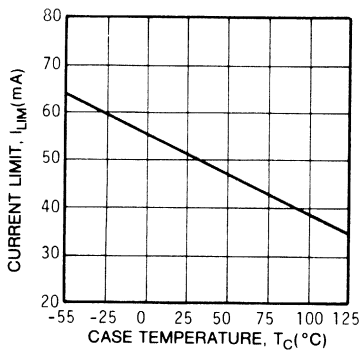
1. Signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. The power supply voltage for all tests is ±150V unless otherwise specified as a test condition.
4. Doubles for every 10°C of temperature increase.
5. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
6. Rating applies if the output current alternates between both output transistors.
7. The internal substrate contains beryllia (BeO). Do not break the hermetic seal. If broken, do not crush, machine or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
8. The PA83M is screened to MIL-STD-883C Class B Method 5008. See military models.

# PA84 TYPICAL PERFORMANCE GRAPHS

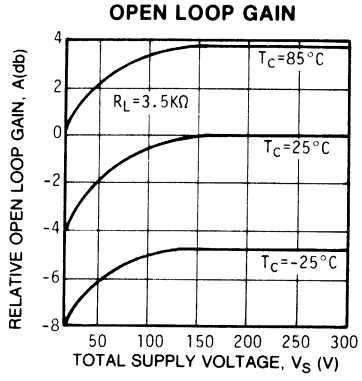
### POWER DERATING



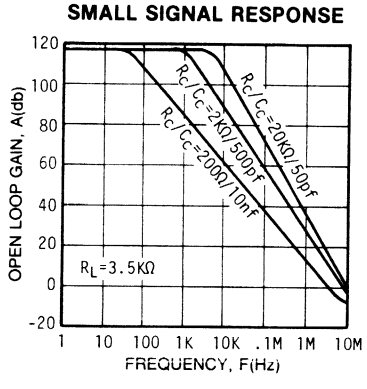

### CURRENT LIMIT



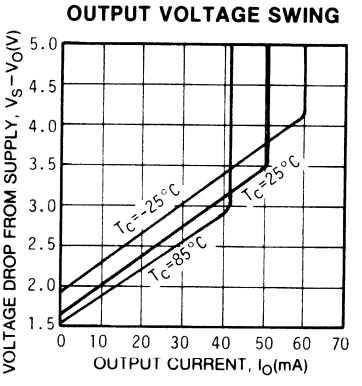

### OPEN LOOP GAIN



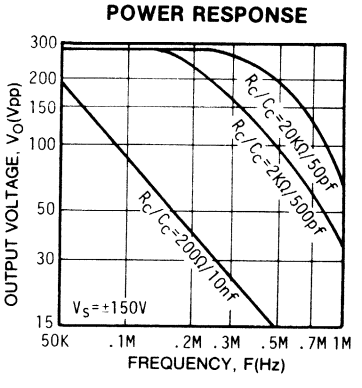

### SMALL SIGNAL RESPONSE



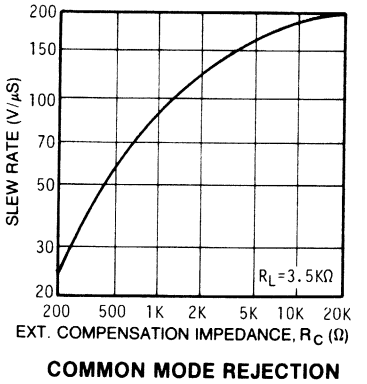

### OUTPUT VOLTAGE SWING



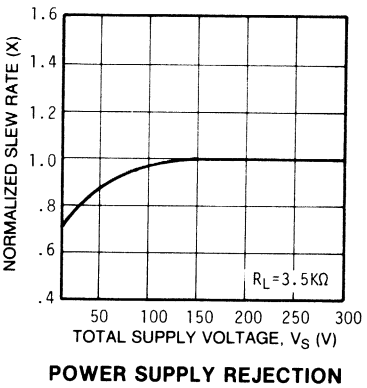

### POWER RESPONSE



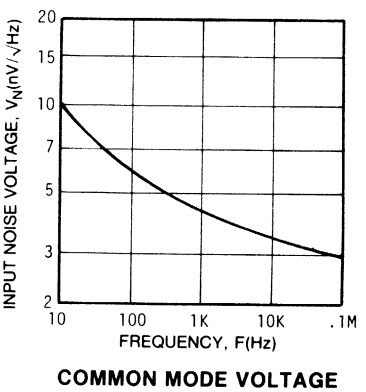

### SLEW RATE VS. COMP.



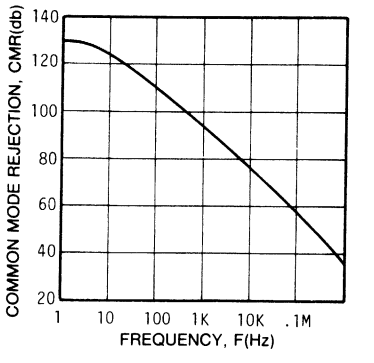

### SLEW RATE VS. SUPPLY



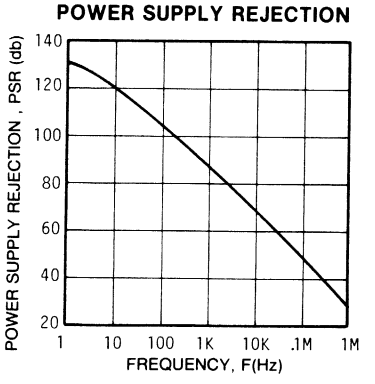

### INPUT NOISE



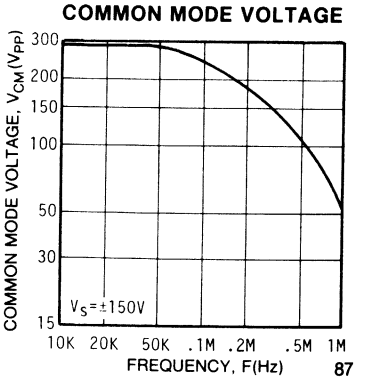

### COMMON MODE REJECTION




### POWER SUPPLY REJECTION




### COMMON MODE VOLTAGE



# PA84 OPERATING CONSIDERATIONS

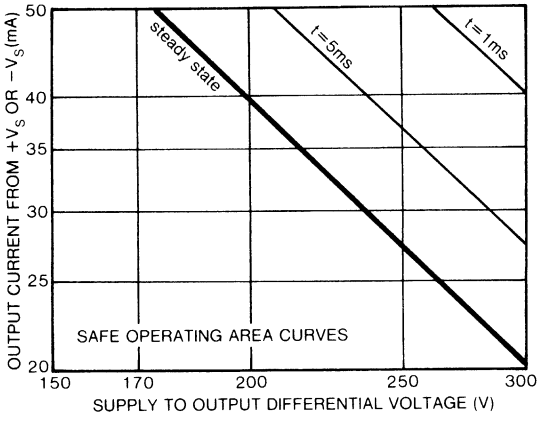
## GENERAL

Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks and mating sockets, see the "Package Outline" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

## SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The secondary breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.




The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. The following capacitive and inductive loads are safe:

| $\pm V_S$ | C(MAX) | L(MAX) |
|---|---|---|
| 150V | 1.2μF | .7H |
| 125V | 6.0μF | 25H |
| 100V | 12μF | 90H |
| 75V | ALL | ALL |

2. Short circuits to ground are safe with dual supplies up to ±150V or single supplies up to 150V.
3. Short circuits to the supply rails are safe with total supply voltages up to 150V. (ie ±75V).

## THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds safe limits. This allows the heatsink design to be based solely on normal conditions but prevents excessive temperatures during abnormal high power conditions without overdesigning the heatsink.

Under abnormal operating conditions, activation of the thermal shutdown is a sign that the internal temperatures have reached approximately 150°. Continued operation in this temperature range will reduce the life of the product. Also, in this operating mode the device may oscillate in and out of thermal shutoff destroying useful signals.

## INDUCTIVE LOADS

Two external diodes as shown in figure 2, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

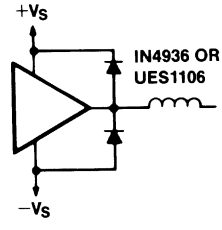



**FIGURE 1. PROTECTIVE, INDUCTIVE LOAD.**

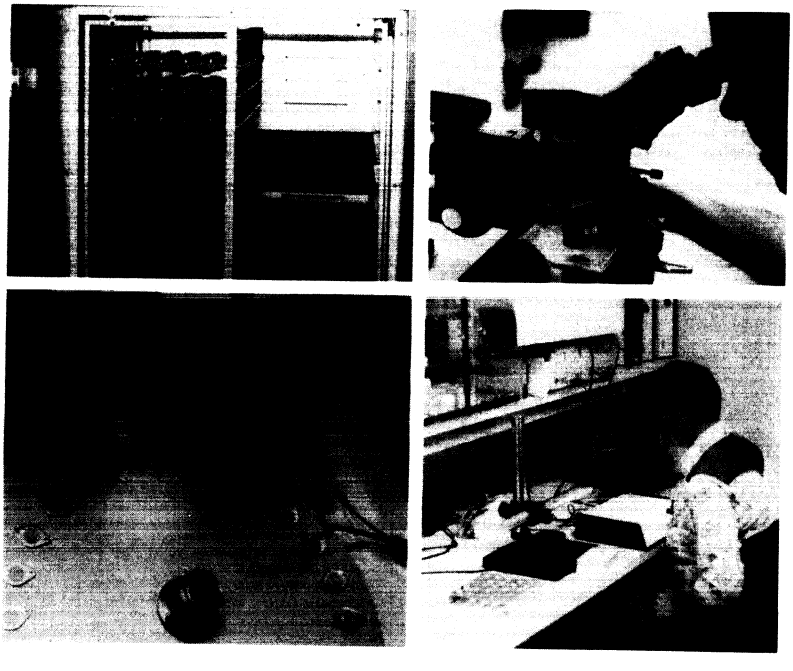
## STABILITY

Due to its large bandwidth the PA84 is more likely to oscillate than lower bandwidth Power Operational Amplifiers such as the PA83 or PA08. To prevent oscillators a reasonable phase margin must be maintained by:

1. Selection of the proper phase compensation capacitor and resistor. Use the values given in the table under external connections on Page 1 and interpolate if necessary. The phase margin can be increased by using a larger capacitor and a smaller resistor than the slew rate optimized values listed in the table. The compensation capacitor may be connected to common (in lieu of $+V_S$) if the positive supply is properly bypassed to common.
2. Keeping the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistance can be used with increased phase compensation (see 1 above)
3. Connecting the amplifier case to a local AC common thus preventing it from acting as an antenna.

# •MILITARY MODELS

***High reliability for critical applications . . .***
***MIL-STD-883C, level B screening***



# PROCESS SPECIFICATIONS
## MIL-STD-883 SCREENED POWER OP AMPS

### CONSTRUCTION

These Power Operational Amplifiers have been built and assembled using the chip and wire process. Fig. 1 shows the manufacturing processes, starting with a metallized ceramic (beryllia substrate) which contains all resistors and conductors for the circuit. The power transistor chips are soldered to silver conductors using low leaching, high temperature solder, the metallized ceramic is also soldered to the header with high temperature solder. All small signal semiconductors and all capacitors are die attached using silver epoxy which is cured at 150°C or higher. The chips have aluminum top metallization pads which are wire bonded to the conductors on the substrate using 1 mil, 5 mil and 10 mil diameter aluminum wire. The package is hermetically sealed using high-speed, one shot resistance welding.

### CLASS B SCREENING

Screened devices are marked with an operator/date code unique to each manufacturing lot. The lot traveler (flow sheet) provides traceability to the components used in that lot. Table 1 outlines all 100% screens/tests performed on each lot, meeting requirements of Method 5008.

### TABLE 1. 100% SCREENS/TESTS

| SCREEN | METHOD | PARAMETER |
|---|---|---|
| Internal Visual | 2017 | Chip quality, workmanship |
| Stabilization Bake | 1008C | 24 Hrs. Bake at 150°C post seal |
| Temp Cycle | 1010C | −65 to +150°C, 10 cycles |
| Acceleration | 2001B | 10,000g, Y1 Axis |
| Interim Electrical | Group A | Subgroups 1 and 4 |
| Burn-In Test | 1015D | 160 Hrs. at 125°C case |
| Final Electrical | Group A | Subgroups 1 thru 6 |
| Fine Leak | 1014A | 1 x $10^{-7}$ cc/sec |
| Gross Leak | 1014C | 60 psi prepressurization |
| External Visual | 2009 | Package appearance, marking |

In addition, the sample tests/screens shown in Table 2 are performed periodically. The water vapor contents test, using a Panametrics Model 771 and chip sensor is traceable to each production lot. No failures are acceptable for these screens.

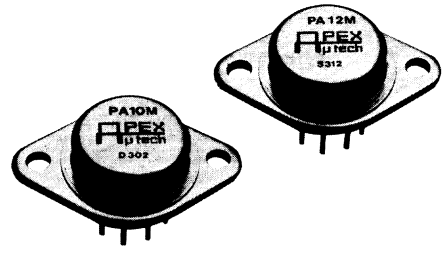
### TABLE 2. SAMPLE TESTS, LOTS

| SCREEN | METHOD | SG | SAMPLE QUANTITY |
|---|---|---|---|
| Physical Dimension | 2016 | 1 | 2 ea. |
| Internal Visual | 2014 | 2 | 1 ea., using reject device |
| Bond Strength | 2011 | 3 | 1 ea., using reject device |
| Water Vapor Contents | see test | 4 | 1 ea., Internal Moisture Sensor |

TO-3 package vendors are qualified by the package related tests outlined in Table 3. The packages are marked with solvent resistant ink. An operating life test is performed after each major change in materials, processes or design, or annually.

### TABLE 3. SAMPLE TESTS, PACKAGE OR PROCESS RELATED

| SCREEN | METHOD | SG | SAMPLE | ACCEPT FAILURES |
|---|---|---|---|---|
| Operating Life Test | 1005 | 1 | 45 | 5 |
| Resist. to Sovlents | 2015 | 2 | 3 | 0 |
| Lead Integrity | 2004B | 2 | 3 | 0 |
| Thermal Shock | 1011B | 3 | 10 | 0 |
| Temp Cycles 100x | 1010C | 3 | 10 | 0 |
| Moisture Resistance | 1004 | 3 | 10 | 0 |
| Salt Atmosphere | 1009 | 5 | 10 | 0 |
| Solderability | 2003 | 6 | 3 | 0 |




### DESCRIPTION

These Power Operational Amplifiers have been screened to MIL-STD-883C, Method 5008, Class B to achieve high reliability and satisfy the requirements for components used in airborne and groundbased military applications. Compliance with these requirements is signified by the "M" suffix in the model number. APEX is working toward and expects to obtain MIL-STD-1772 certification by November 1986.

The specifications and performances are similar to the industrial grade standard model (no suffix). However, all specifications listed in the Group A inspection table on individual model data sheets have been tested over the full military temperature range of −55°C to 125°C. To find additional specifications and the performance graphs, please consult the data sheet for the standard model number. The package outline is identical but the pins are gold plated to meet the solderability of Method 2003 MIL-STD-883C.

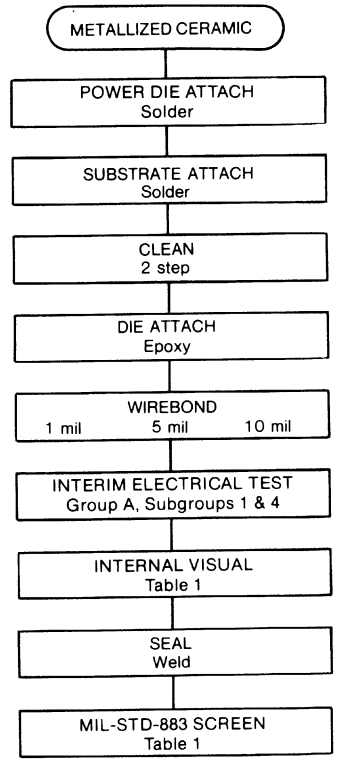
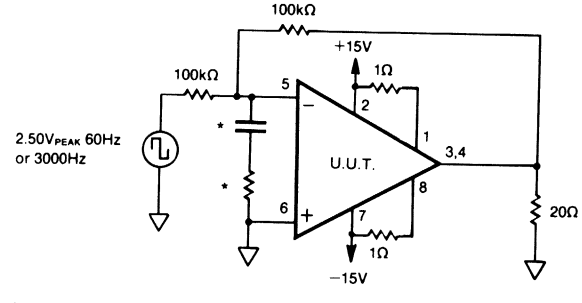



**FIG. 1 MANUFACTURING FLOW**

## TABLE 4 — GROUP A INSPECTION

| SG | PARAMETER | SYMBOL | TEMP | PWR | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| 1 | Quiescent Current | $I_Q$ | 25°C | ±15V | $V_{IN}$ = 0, G = 100 | | 40 | mA |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±15V | $V_{IN}$ = 0, G = 100 | | 10 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±7V | $V_{IN}$ = 0, G = 100 | | 11.6 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±19V | $V_{IN}$ = 0, G = 100 | | 10.8 | mV |
| 1 | Input Bias Current, +IN | $+I_B$ | 25°C | ±15V | $V_{IN}$ = 0, G = 100 | | 200 | pA |
| 1 | Input Bias Current, −IN | $-I_B$ | 25°C | ±15V | $V_{IN}$ = 0, G = 100 | | 200 | pA |
| 1 | Input Offset Current | $I_{OS}$ | 25°C | ±15V | $V_{IN}$ = 0, G = 100 | | 100 | pA |
| 3 | Quiescent Current | $I_Q$ | −55°C | ±15V | $V_{IN}$ = 0, G = 100 | | 200 | mA |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±15V | $V_{IN}$ = 0, G = 100 | | 14 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±7V | $V_{IN}$ = 0, G = 100 | | 15.6 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±19V | $V_{IN}$ = 0, G = 100 | | 14.8 | mV |
| 3 | Input Bias Current, +IN | $+I_B$ | −55°C | ±15V | $V_{IN}$ = 0, G = 100 | | 200 | pA |
| 3 | Input Bias Current, −IN | $-I_B$ | −55°C | ±15V | $V_{IN}$ = 0, G = 100 | | 200 | pA |
| 3 | Input Offset Current | $I_{OS}$ | −55°C | ±15V | $V_{IN}$ = 0, G = 100 | | 100 | pA |
| 2 | Quiescent Current | $I_Q$ | 125°C | ±15V | $V_{IN}$ = 0, G = 100 | | 60 | mA |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±15V | $V_{IN}$ = 0, G = 100 | | 15 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±7V | $V_{IN}$ = 0, G = 100 | | 16.6 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±19V | $V_{IN}$ = 0, G = 100 | | 15.8 | mV |
| 2 | Input Bias Current, +IN | $+I_B$ | 125°C | ±15V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Bias Current, −IN | $-I_B$ | 125°C | ±15V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Offset Current | $I_{OS}$ | 125°C | ±15V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 4 | Output Voltage, $I_O$ = 5A | $V_O$ | 25°C | ±9V | $R_L$ = 1Ω | 5 | | V |
| 4 | Output Voltage, $I_O$ = 36mA | $V_O$ | 25°C | ±19V | $R_L$ = 500Ω | 18 | | V |
| 4 | Output Voltage, $I_O$ = 2A | $V_O$ | 25°C | ±12V | $R_L$ = 5Ω | 10 | | V |
| 4 | Current Limits | $I_{CL}$ | 25°C | ±9V | $R_L$ = 1Ω, $R_{CL}$ = .2Ω | 2.6 | 3.9 | A |
| 4 | Stability/Noise | $E_N$ | 25°C | ±15V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 4 | Slew Rate | SR | 25°C | ±18V | $R_L$ = 500Ω | 13 | 100 | V/µs |
| 4 | Open Loop Gain | $A_{OL}$ | 25°C | ±15V | $R_L$ = 500Ω, f = 10Hz | 86 | | db |
| 4 | Common-mode Rejection | CMR | 25°C | ±8.25V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±2.25V | 70 | | db |
| 6 | Output Voltage, $I_O$ = 5A | $V_O$ | −55°C | ±9V | $R_L$ = 1Ω | 5 | | V |
| 6 | Output Voltage, $I_O$ = 36mA | $V_O$ | −55°C | ±19V | $R_L$ = 500Ω | 18 | | V |
| 6 | Output Voltage, $I_O$ = 2A | $V_O$ | −55°C | ±12V | $R_L$ = 5Ω | 10 | | V |
| 6 | Stability/Noise | $E_N$ | −55°C | ±15V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 6 | Slew Rate | SR | −55°C | ±18V | $R_L$ = 500Ω | 13 | 100 | V/µs |
| 6 | Open Loop Gain | $A_{OL}$ | −55°C | ±15V | $R_L$ = 500Ω, f = 10Hz | 86 | | db |
| 6 | Common-mode Rejection | CMR | −55°C | ±8.25V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±2.25V | 70 | | db |
| 5 | Output Voltage, $I_O$ = 3A | $V_O$ | 125°C | ±7V | $R_L$ = 1Ω | 3 | | V |
| 5 | Output Voltage, $I_O$ = 36mA | $V_O$ | 125°C | ±19V | $R_L$ = 500Ω | 18 | | V |
| 5 | Output Voltage, $I_O$ = 2A | $V_O$ | 125°C | ±12V | $R_L$ = 5Ω | 10 | | V |
| 5 | Stability/Noise | $E_N$ | 125°C | ±15V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 5 | Slew Rate | SR | 125°C | ±18V | $R_L$ = 500Ω | 8.5 | 100 | V/µs |
| 5 | Open Loop Gain | $A_{OL}$ | 125°C | ±15V | $R_L$ = 500Ω, f = 10Hz | 86 | | db |
| 5 | Common-mode Rejection | CMR | 125°C | ±8.25V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±2.25V | 70 | | db |

**BURN IN CIRCUIT:**



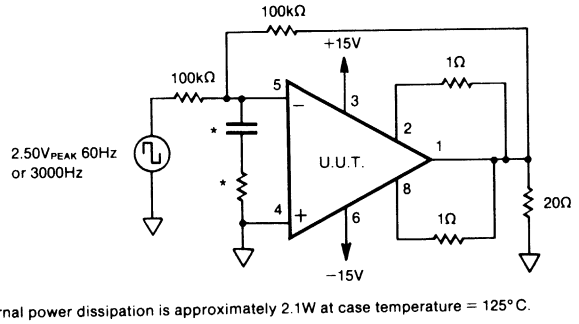

Internal power dissipation is approximately 2.1W at case temperature = 125°C.

*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

## TABLE 4 — GROUP A INSPECTION

| SG | PARAMETER | SYMBOL | TEMP | PWR | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| 1 | Quiescent Current | $I_Q$ | 25°C | ±35V | $V_{IN}$ = 0, G = 100 | | 30 | mA |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±35V | $V_{IN}$ = 0, G = 100 | | 2 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±12V | $V_{IN}$ = 0, G = 100 | | 4.3 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±50V | $V_{IN}$ = 0, G = 100 | | 3.5 | mV |
| 1 | Input Bias Current, +IN | $+I_B$ | 25°C | ±35V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 1 | Input Bias Current, −IN | $-I_B$ | 25°C | ±35V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 1 | Input Offset Current | $I_{OS}$ | 25°C | ±35V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Quiescent Current | $I_Q$ | −55°C | ±35V | $V_{IN}$ = 0, G = 100 | | 46 | mA |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±35V | $V_{IN}$ = 0, G = 100 | | 4.4 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±12V | $V_{IN}$ = 0, G = 100 | | 6.7 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±50V | $V_{IN}$ = 0, G = 100 | | 5.9 | mV |
| 3 | Input Bias Current, +IN | $+I_B$ | −55°C | ±35V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Input Bias Current, −IN | $-I_B$ | −55°C | ±35V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Input Offset Current | $I_{OS}$ | −55°C | ±35V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 2 | Quiescent Current | $I_Q$ | 125°C | ±35V | $V_{IN}$ = 0, G = 100 | | 30 | mA |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±35V | $V_{IN}$ = 0, G = 100 | | 5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±12V | $V_{IN}$ = 0, G = 100 | | 7.3 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±50V | $V_{IN}$ = 0, G = 100 | | 6.5 | mV |
| 2 | Input Bias Current, +IN | $+I_B$ | 125°C | ±35V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Bias Current, −IN | $-I_B$ | 125°C | ±35V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Offset Current | $I_{OS}$ | 125°C | ±35V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 4 | Output Voltage, $I_O$ = 5A | $V_O$ | 25°C | ±15.3V | $R_L$ = 2.07Ω | 10.3 | | V |
| 4 | Output Voltage, $I_O$ = 90mA | $V_O$ | 25°C | ±50V | $R_L$ = 500Ω | 45 | | V |
| 4 | Output Voltage, $I_O$ = 2A | $V_O$ | 25°C | ±29V | $R_L$ = 12Ω | 24 | | V |
| 4 | Current Limits | $I_{CL}$ | 25°C | ±16V | $R_L$ = 2.07Ω, $R_{CL}$ = .2Ω | 2.6 | 3.9 | A |
| 4 | Stability/Noise | $E_N$ | 25°C | ±35V | $R_L$ = 500Ω, G = 1, $C_L$ = 10nF | | 1 | mV |
| 4 | Slew Rate | SR | 25°C | ±35V | $R_L$ = 500Ω | 2.5 | 10 | V/μs |
| 4 | Open Loop Gain | $A_{OL}$ | 25°C | ±35V | $R_L$ = 500Ω, f = 10Hz | 92 | | db |
| 4 | Common-mode Rejection | CMR | 25°C | ±34.5V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±22.5V | 80 | | db |
| 6 | Output Voltage, $I_O$ = 5A | $V_O$ | −55°C | ±15.3V | $R_L$ = 2.07Ω | 10.3 | | V |
| 6 | Output Voltage, $I_O$ = 90mA | $V_O$ | −55°C | ±50V | $R_L$ = 500Ω | 45 | | V |
| 6 | Output Voltage, $I_O$ = 2A | $V_O$ | −55°C | ±29V | $R_L$ = 12Ω | 24 | | V |
| 6 | Stability/Noise | $E_N$ | −55°C | ±35V | $R_L$ = 500Ω, G = 1, $C_L$ = 10nF | | 1 | mV |
| 6 | Slew Rate | SR | −55°C | ±35V | $R_L$ = 500Ω | 2.5 | 10 | V/μs |
| 6 | Open Loop Gain | $A_{OL}$ | −55°C | ±35V | $R_L$ = 500Ω, f = 10Hz | 92 | | db |
| 6 | Common-mode Rejection | CMR | −55°C | ±34.5V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±22.5V | 80 | | db |
| 5 | Output Voltage, $I_O$ = 3A | $V_O$ | 125°C | ±11.3V | $R_L$ = 2.07Ω | 6.3 | | V |
| 5 | Output Voltage, $I_O$ = 90mA | $V_O$ | 125°C | ±50V | $R_L$ = 500Ω | 45 | | V |
| 5 | Output Voltage, $I_O$ = 2A | $V_O$ | 125°C | ±29V | $R_L$ = 12Ω | 24 | | V |
| 5 | Stability/Noise | $E_N$ | 125°C | ±35V | $R_L$ = 500Ω, G = 1, $C_L$ = 10nF | | 1 | mV |
| 5 | Slew Rate | SR | 125°C | ±35V | $R_L$ = 500Ω | 1.25 | 10 | V/μs |
| 5 | Open Loop Gain | $A_{OL}$ | 125°C | ±35V | $R_L$ = 500Ω, f = 10Hz | 92 | | db |
| 5 | Common-mode Rejection | CMR | 125°C | ±34.5V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±22.5V | 80 | | db |

**BURN IN CIRCUIT:**



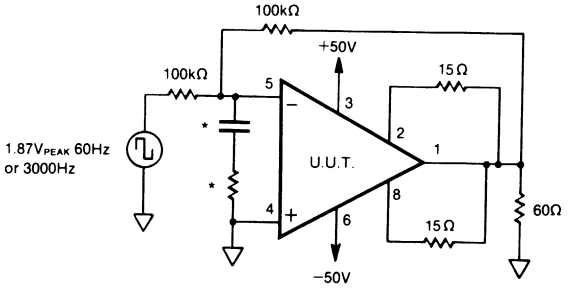

Internal power dissipation is approximately 2.1W at case temperature = 125°C.

*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

## TABLE 4 — GROUP A INSPECTION

| SG | PARAMETER | SYMBOL | TEMP | PWR | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| 1 | Quiescent Current | $I_Q$ | 25°C | ±100V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = 6.5Ω | | 8.5 | mA |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±100V | $V_{IN}$ = 0, G = 100 | | 2 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±15V | $V_{IN}$ = 0, G = 100 | | 3.7 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±150V | $V_{IN}$ = 0, G = 100 | | 3 | mV |
| 1 | Input Bias Current, +IN | $+I_B$ | 25°C | ±100V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 1 | Input Bias Current, −IN | $-I_B$ | 25°C | ±100V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 1 | Input Offset Current | $I_{OS}$ | 25°C | ±100V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Quiescent Current | $I_Q$ | −55°C | ±100V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = 6.5Ω | | 9.5 | mA |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±100V | $V_{IN}$ = 0, G = 100 | | 4.4 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±15V | $V_{IN}$ = 0, G = 100 | | 6.1 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±150V | $V_{IN}$ = 0, G = 100 | | 5.4 | mV |
| 3 | Input Bias Current, +IN | $+I_B$ | −55°C | ±100V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Input Bias Current, −IN | $-I_B$ | −55°C | ±100V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Input Offset Current | $I_{OS}$ | −55°C | ±100V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 2 | Quiescent Current | $I_Q$ | 125°C | ±100V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = 6.5Ω | | 11 | mA |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±100V | $V_{IN}$ = 0, G = 100 | | 5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±15V | $V_{IN}$ = 0, G = 100 | | 6.7 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±150V | $V_{IN}$ = 0, G = 100 | | 6 | mV |
| 2 | Input Bias Current, +IN | $+I_B$ | 125°C | ±100V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Bias Current, −IN | $-I_B$ | 125°C | ±100V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Offset Current | $I_{OS}$ | 125°C | ±100V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 4 | Output Voltage, $I_O$ = 150mA | $V_O$ | 25°C | ±31V | $R_L$ = 100Ω, $R_{CL}$ = 1.8Ω | 15 | | V |
| 4 | Output Voltage, $I_O$ = 29mA | $V_O$ | 25°C | ±150V | $R_L$ = 5K, $R_{CL}$ = 6.5Ω | 145 | | V |
| 4 | Output Voltage, $I_O$ = 80mA | $V_O$ | 25°C | ±90V | $R_L$ = 1K, $R_{CL}$ = 1.8Ω | 80 | | V |
| 4 | Current Limits | $I_{CL}$ | 25°C | ±30V | $R_L$ = 100Ω, $R_{CL}$ = 6.5Ω | 75 | 110 | mA |
| 4 | Stability/Noise | $E_N$ | 25°C | ±100V | $R_L$ = 5K, G = 1, $C_L$ = 10nF | | 1 | mV |
| 4 | Slew Rate | SR | 25°C | ±100V | $R_L$ = 5K | 20 | 100 | V/μs |
| 4 | Open Loop Gain | $A_{OL}$ | 25°C | ±100V | $R_L$ = 5K, f = 10Hz | 96 | | db |
| 4 | Common-mode Rejection | CMR | 25°C | ±32.5V | $R_L$ = 5K, f = DC, $V_{CM}$ = ±22.5V | 90 | | db |
| 6 | Output Voltage, $I_O$ = 100mA | $V_O$ | −55°C | ±31V | $R_L$ = 100Ω, $R_{CL}$ = 1.8Ω | 10 | | V |
| 6 | Output Voltage, $I_O$ = 29mA | $V_O$ | −55°C | ±150V | $R_L$ = 5K, $R_{CL}$ = 6.5Ω | 145 | | V |
| 6 | Output Voltage, $I_O$ = 70mA | $V_O$ | −55°C | ±90V | $R_L$ = 1K, $R_{CL}$ = 1.8Ω | 70 | | V |
| 6 | Stability/Noise | $E_N$ | −55°C | ±100V | $R_L$ = 5K, G = 1, $C_L$ = 10nF | | 1 | mV |
| 6 | Slew Rate | SR | −55°C | ±100V | $R_L$ = 5K | 20 | 100 | V/μs |
| 6 | Open Loop Gain | $A_{OL}$ | −55°C | ±100V | $R_L$ = 5K, f = 10Hz | 96 | | db |
| 6 | Common-mode Rejection | CMR | −55°C | ±32.5V | $R_L$ = 5K, f = DC, $V_{CM}$ = ±22.5V | 90 | | db |
| 5 | Output Voltage, $I_O$ = 150mA | $V_O$ | 125°C | ±31V | $R_L$ = 100Ω, $R_{CL}$ = 1.8Ω | 15 | | V |
| 5 | Output Voltage, $I_O$ = 29mA | $V_O$ | 125°C | ±150V | $R_L$ = 5K, $R_{CL}$ = 6.5Ω | 145 | | V |
| 5 | Output Voltage, $I_O$ = 80mA | $V_O$ | 125°C | ±90V | $R_L$ = 1K, $R_{CL}$ = 1.8Ω | 80 | | V |
| 5 | Stability/Noise | $E_N$ | 125°C | ±150V | $R_L$ = 5K, G = 1, $C_L$ = 10nF | | 1 | mV |
| 5 | Slew Rate | SR | 125°C | ±150V | $R_L$ = 5K | 20 | 100 | V/μs |
| 5 | Open Loop Gain | $A_{OL}$ | 125°C | ±150V | $R_L$ = 5K, f = 10Hz | 96 | | db |
| 5 | Common-mode Rejection | CMR | 125°C | ±32.5V | $R_L$ = 5K, f = DC, $V_{CM}$ = ±22.5V | 90 | | db |

**BURN IN CIRCUIT:**



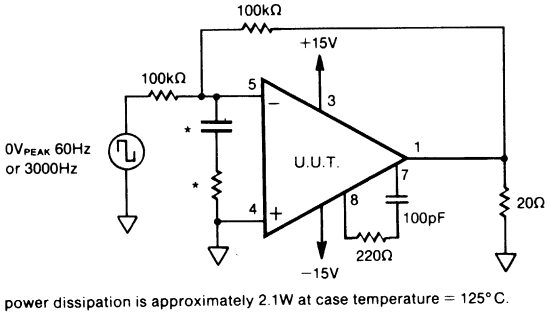

Internal power dissipation is approximately 2.1W at case temperature = 125°C.

*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

## TABLE 4 — GROUP A INSPECTION

| SG | PARAMETER | SYMBOL | TEMP | PWR | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| 1 | Quiescent Current | $I_Q$ | 25°C | ±35V | $V_{IN}$ = 0, G = 100 | | 85 | mA |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±35V | $V_{IN}$ = 0, G = 100 | | 3 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±12V | $V_{IN}$ = 0, G = 100 | | 5.3 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100 | | 3.5 | mV |
| 1 | Input Bias Current, +IN | $+I_B$ | 25°C | ±35V | $V_{IN}$ = 0, G = 100 | | 100 | pA |
| 1 | Input Bias Current, −IN | $-I_B$ | 25°C | ±35V | $V_{IN}$ = 0, G = 100 | | 100 | pA |
| 1 | Input Offset Current | $I_{OS}$ | 25°C | ±35V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Quiescent Current | $I_Q$ | −55°C | ±35V | $V_{IN}$ = 0, G = 100 | | 165 | mA |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±35V | $V_{IN}$ = 0, G = 100 | | 5.4 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±12V | $V_{IN}$ = 0, G = 100 | | 7.7 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100 | | 5.9 | mV |
| 3 | Input Bias Current, +IN | $+I_B$ | −55°C | ±35V | $V_{IN}$ = 0, G = 100 | | 100 | pA |
| 3 | Input Bias Current, −IN | $-I_B$ | −55°C | ±35V | $V_{IN}$ = 0, G = 100 | | 100 | pA |
| 3 | Input Offset Current | $I_{OS}$ | −55°C | ±35V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 2 | Quiescent Current | $I_Q$ | 125°C | ±35V | $V_{IN}$ = 0, G = 100 | | 140 | mA |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±35V | $V_{IN}$ = 0, G = 100 | | 6 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±12V | $V_{IN}$ = 0, G = 100 | | 8.3 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100 | | 6.5 | mV |
| 2 | Input Bias Current, +IN | $+I_B$ | 125°C | ±35V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Bias Current, −IN | $-I_B$ | 125°C | ±35V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Offset Current | $I_{OS}$ | 125°C | ±35V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 4 | Output Voltage, $I_O$ = 3A | $V_O$ | 25°C | ±21.3V | $R_L$ = 3.75Ω | 11.3 | | V |
| 4 | Output Voltage, $I_O$ = 66mA | $V_O$ | 25°C | ±40V | $R_L$ = 500Ω | 33 | | V |
| 4 | Output Voltage, $I_O$ = 2A | $V_O$ | 25°C | ±38V | $R_L$ = 15Ω | 30 | | V |
| 4 | Current Limits | $I_{CL}$ | 25°C | ±32.2V | $R_L$ = 3.75Ω | 3.4 | 6 | A |
| 4 | Stability/Noise | $E_N$ | 25°C | ±35V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 4 | Slew Rate | SR | 25°C | ±35V | $R_L$ = 500Ω, G = 1 | 25 | 500 | V/μs |
| 4 | Open Loop Gain | $A_{OL}$ | 25°C | ±35V | $R_L$ = 500Ω, f = 10Hz | 80 | | db |
| 4 | Common-mode Rejection | CMR | 25°C | ±34.5V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±22.5V | 64 | | db |
| 6 | Output Voltage, $I_O$ = 3A | $V_O$ | −55°C | ±21.3V | $R_L$ = 3.75Ω | 11.3 | | V |
| 6 | Output Voltage, $I_O$ = 66mA | $V_O$ | −55°C | ±40V | $R_L$ = 500Ω | 33 | | V |
| 6 | Output Voltage, $I_O$ = 2A | $V_O$ | −55°C | ±38V | $R_L$ = 15Ω | 30 | | V |
| 6 | Stability/Noise | $E_N$ | −55°C | ±35V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 6 | Slew Rate | SR | −55°C | ±35V | $R_L$ = 500Ω, G = 1 | 25 | 500 | V/μs |
| 6 | Open Loop Gain | $A_{OL}$ | −55°C | ±35V | $R_L$ = 500Ω, f = 10Hz | 80 | | db |
| 6 | Common-mode Rejection | CMR | −55°C | ±34.5V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±22.5V | 64 | | db |
| 5 | Output Voltage, $I_O$ = 1A | $V_O$ | 125°C | ±14V | $R_L$ = 3.75Ω | 3.75 | | V |
| 5 | Output Voltage, $I_O$ = 66mA | $V_O$ | 125°C | ±40V | $R_L$ = 500Ω | 33 | | V |
| 5 | Output Voltage, $I_O$ = 1A | $V_O$ | 125°C | ±23.5V | $R_L$ = 15Ω | 15 | | V |
| 5 | Stability/Noise | $E_N$ | 125°C | ±35V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 5 | Slew Rate | SR | 125°C | ±35V | $R_L$ = 500Ω, G = 1 | 20 | 500 | V/μs |
| 5 | Open Loop Gain | $A_{OL}$ | 125°C | ±35V | $R_L$ = 500Ω, f = 10Hz | 80 | | db |
| 5 | Common-mode Rejection | CMR | 125°C | ±34.5V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±22.5V | 64 | | db |

### BURN IN CIRCUIT:



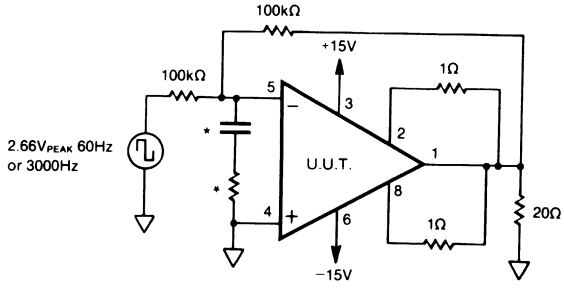

Internal power dissipation is approximately 2.1W at case temperature = 125°C.

*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

## TABLE 4 — GROUP A INSPECTION

| SG | PARAMETER | SYMBOL | TEMP | PWR | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| 1 | Quiescent Current | $I_Q$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = .1Ω | | 30 | mA |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±6 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±12 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±45V | $V_{IN}$ = 0, G = 100 | | ±7 | mV |
| 1 | Input Bias Current, +IN | $+I_B$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±30 | nA |
| 1 | Input Bias Current, −IN | $-I_B$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±30 | nA |
| 1 | Input Offset Current | $I_{OS}$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±30 | nA |
| 3 | Quiescent Current | $I_Q$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = .1Ω | | 75 | mA |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±11.2 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±17.2 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±45V | $V_{IN}$ = 0, G = 100 | | ±12.2 | mV |
| 3 | Input Bias Current, +IN | $+I_B$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±62 | nA |
| 3 | Input Bias Current, −IN | $-I_B$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±62 | nA |
| 3 | Input Offset Current | $I_{OS}$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±62 | nA |
| 2 | Quiescent Current | $I_Q$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = .1Ω | | 30 | mA |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±12.5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±18.5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±45V | $V_{IN}$ = 0, G = 100 | | ±13.5 | mV |
| 2 | Input Bias Current, +IN | $+I_B$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±70 | nA |
| 2 | Input Bias Current, −IN | $-I_B$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±70 | nA |
| 2 | Input Offset Current | $I_{OS}$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±70 | nA |
| 4 | Output Voltage, $I_O$ = 5A | $V_O$ | 25°C | ±18V | $R_L$ = 2.07Ω | 10 | | V |
| 4 | Output Voltage, $I_O$ = 80mA | $V_O$ | 25°C | ±45V | $R_L$ = 500Ω | 40 | | V |
| 4 | Output Voltage, $I_O$ = 2A | $V_O$ | 25°C | ±30V | $R_L$ = 12Ω | 24 | | V |
| 4 | Current Limits | $I_{CL}$ | 25°C | ±16.5V | $R_L$ = 2.07Ω, $R_{CL}$ = .2Ω | 2.6 | 3.9 | A |
| 4 | Stability/Noise | $E_N$ | 25°C | ±40V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 4 | Slew Rate | SR | 25°C | ±40V | $R_L$ = 500Ω | 2.5 | 10 | V/μs |
| 4 | Open Loop Gain | $A_{OL}$ | 25°C | ±40V | $R_L$ = 500Ω, f = 10Hz | 96 | | db |
| 4 | Common-mode Rejection | CMR | 25°C | +15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 74 | | db |
| 6 | Output Voltage, $I_O$ = 5A | $V_O$ | −55°C | ±18V | $R_L$ = 2.07Ω | 10 | | V |
| 6 | Output Voltage, $I_O$ = 80mA | $V_O$ | −55°C | ±45V | $R_L$ = 500Ω | 40 | | V |
| 6 | Output Voltage, $I_O$ = 2A | $V_O$ | −55°C | ±30V | $R_L$ = 12Ω | 24 | | V |
| 6 | Stability/Noise | $E_N$ | −55°C | ±40V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 6 | Slew Rate | SR | −55°C | ±40V | $R_L$ = 500Ω | 2.5 | 10 | V/μs |
| 6 | Open Loop Gain | $A_{OL}$ | −55°C | ±40V | $R_L$ = 500Ω, f = 10Hz | 96 | | db |
| 6 | Common-mode Rejection | CMR | −55°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 74 | | db |
| 5 | Output Voltage, $I_O$ = 3A | $V_O$ | 125°C | ±14.3V | $R_L$ = 2.07Ω | 6.3 | | V |
| 5 | Output Voltage, $I_O$ = 80mA | $V_O$ | 125°C | ±45V | $R_L$ = 500Ω | 40 | | V |
| 5 | Output Voltage, $I_O$ = 2A | $V_O$ | 125°C | ±30V | $R_L$ = 12Ω | 24 | | V |
| 5 | Stability/Noise | $E_N$ | 125°C | ±40V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 5 | Slew Rate | SR | 125°C | ±40V | $R_L$ = 500Ω | 2.5 | 10 | V/μs |
| 5 | Open Loop Gain | $A_{OL}$ | 125°C | ±40V | $R_L$ = 500Ω, f = 10Hz | 96 | | db |
| 5 | Common-mode Rejection | CMR | 125°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 74 | | db |

## BURN IN CIRCUIT:



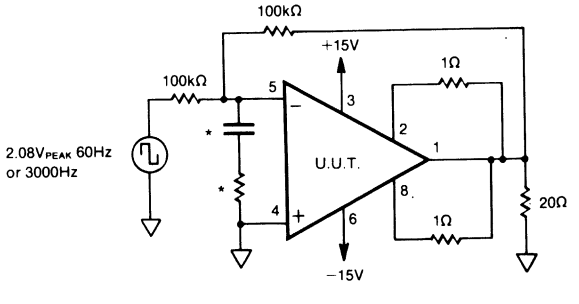

Internal power dissipation is approximately 2.1W at case temperature = 125°C.

*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

## TABLE 4 — GROUP A INSPECTION

| SG | PARAMETER | SYMBOL | TEMP | PWR | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| 1 | Quiescent Current | $I_Q$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = .1Ω | | 50 | mA |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±6 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±12 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±45V | $V_{IN}$ = 0, G = 100 | | ±7 | mV |
| 1 | Input Bias Current, +IN | $+I_B$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±30 | nA |
| 1 | Input Bias Current, −IN | $-I_B$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±30 | nA |
| 1 | Input Offset Current | $I_{OS}$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±30 | nA |
| 3 | Quiescent Current | $I_Q$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = .1Ω | | 100 | mA |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±11.2 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±17.2 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±45V | $V_{IN}$ = 0, G = 100 | | ±12.2 | mV |
| 3 | Input Bias Current, +IN | $+I_B$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±62 | nA |
| 3 | Input Bias Current, −IN | $-I_B$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±62 | nA |
| 3 | Input Offset Current | $I_{OS}$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±62 | nA |
| 2 | Quiescent Current | $I_Q$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = .1Ω | | 50 | mA |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±12.5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±18.5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±45V | $V_{IN}$ = 0, G = 100 | | ±13.5 | mV |
| 2 | Input Bias Current, +IN | $+I_B$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±70 | nA |
| 2 | Input Bias Current, −IN | $-I_B$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±70 | nA |
| 2 | Input Offset Current | $I_{OS}$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±70 | nA |
| 4 | Output Voltage, $I_O$ = 10A | $V_O$ | 25°C | ±16V | $R_L$ = 1Ω | 10 | | V |
| 4 | Output Voltage, $I_O$ = 80mA | $V_O$ | 25°C | ±45V | $R_L$ = 500Ω | 40 | | V |
| 4 | Output Voltage, $I_O$ = 5A | $V_O$ | 25°C | ±35V | $R_L$ = 6Ω | 30 | | V |
| 4 | Current Limits | $I_{CL}$ | 25°C | ±14V | $R_L$ = 1Ω, $R_{CL}$ = .1Ω | 5 | 7.9 | A |
| 4 | Stability/Noise | $E_N$ | 25°C | ±15V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 4 | Slew Rate | SR | 25°C | ±40V | $R_L$ = 500Ω | 2.5 | 10 | V/µs |
| 4 | Open Loop Gain | $A_{OL}$ | 25°C | ±40V | $R_L$ = 500Ω, f = 10Hz | 96 | | db |
| 4 | Common-mode Rejection | CMR | 25°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 74 | | db |
| 6 | Output Voltage, $I_O$ = 10A | $V_O$ | −55°C | ±16V | $R_L$ = 1Ω | 10 | | V |
| 6 | Output Voltage, $I_O$ = 80mA | $V_O$ | −55°C | ±45V | $R_L$ = 500Ω | 40 | | V |
| 6 | Stability/Noise | $E_N$ | −55°C | ±40V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 6 | Slew Rate | SR | −55°C | ±40V | $R_L$ = 500Ω | 2.5 | 10 | V/µs |
| 6 | Open Loop Gain | $A_{OL}$ | −55°C | ±40V | $R_L$ = 500Ω, f = 10Hz | 96 | | db |
| 6 | Common-mode Rejection | CMR | −55°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 74 | | db |
| 5 | Output Voltage, $I_O$ = 8A | $V_O$ | 125°C | ±14V | $R_L$ = 1Ω | 8 | | V |
| 5 | Output Voltage, $I_O$ = 80mA | $V_O$ | 125°C | ±45V | $R_L$ = 500Ω | 40 | | V |
| 5 | Stability/Noise | $E_N$ | 125°C | ±40V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 5 | Slew Rate | SR | 125°C | ±40V | $R_L$ = 500Ω | 2.5 | 10 | V/µs |
| 5 | Open Loop Gain | $A_{OL}$ | 125°C | ±40V | $R_L$ = 500Ω, f = 10Hz | 96 | | db |
| 5 | Common-mode Rejection | CMR | 125°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 74 | | db |

## BURN IN CIRCUIT:



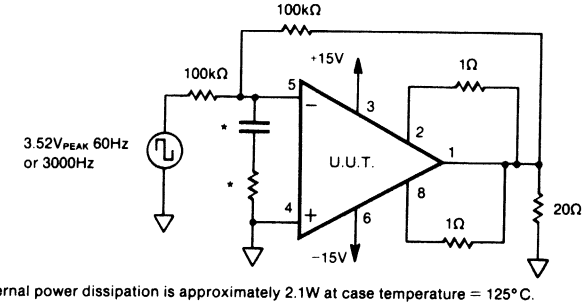

Internal power dissipation is approximately 2.1W at case temperature = 125°C.

*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

## TABLE 4 — GROUP A INSPECTION

| SG | PARAMETER | SYMBOL | TEMP | PWR | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| 1 | Quiescent Current | $I_Q$ | 25°C | ±34V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = .1Ω | | 10 | mA |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±10 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±16 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±11.2 | mV |
| 1 | Input Bias Current, +IN | $+I_B$ | 25°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±40 | nA |
| 1 | Input Bias Current, −IN | $-I_B$ | 25°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±40 | nA |
| 1 | Input Offset Current | $I_{OS}$ | 25°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±10 | nA |
| 3 | Quiescent Current | $I_Q$ | −55°C | ±34V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = .1Ω | | 10 | mA |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±15.2 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±21.2 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±16.4 | mV |
| 3 | Input Bias Current, +IN | $+I_B$ | −55°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±72 | nA |
| 3 | Input Bias Current, −IN | $-I_B$ | −55°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±72 | nA |
| 3 | Input Offset Current | $I_{OS}$ | −55°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±26 | nA |
| 2 | Quiescent Current | $I_Q$ | 125°C | ±34V | $V_{IN}$ = 0, G = 100, $R_{CL}$ = .1Ω | | 13 | mA |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±16.5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±22.5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±40V | $V_{IN}$ = 0, G = 100 | | ±17.7 | mV |
| 2 | Input Bias Current, +IN | $+I_B$ | 125°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±80 | nA |
| 2 | Input Bias Current, −IN | $-I_B$ | 125°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±80 | nA |
| 2 | Input Offset Current | $I_{OS}$ | 125°C | ±34V | $V_{IN}$ = 0, G = 100 | | ±30 | nA |
| 4 | Output Voltage, $I_O$ = 10A | $V_O$ | 25°C | ±18V | $R_L$ = 1Ω | 10 | | V |
| 4 | Output Voltage, $I_O$ = 68mA | $V_O$ | 25°C | ±40V | $R_L$ = 500Ω | 34 | | V |
| 4 | Output Voltage, $I_O$ = 4A | $V_O$ | 25°C | ±30V | $R_L$ = 6Ω | 24 | | V |
| 4 | Current Limits | $I_{CL}$ | 25°C | ±16V | $R_L$ = 1Ω, $R_{CL}$ = .1Ω | 5 | 7.9 | A |
| 4 | Stability/Noise | $E_N$ | 25°C | ±34V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 4 | Slew Rate | SR | 25°C | ±34V | $R_L$ = 500Ω | 1.0 | 10 | V/μs |
| 4 | Open Loop Gain | $A_{OL}$ | 25°C | ±34V | $R_L$ = 500Ω, f = 10Hz | 94 | | db |
| 4 | Common-mode Rejection | CMR | 25°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 70 | | db |
| 6 | Output Voltage, $I_O$ = 10A | $V_O$ | −55°C | ±18V | $R_L$ = 1Ω | 10 | | V |
| 6 | Output Voltage, $I_O$ = 68mA | $V_O$ | −55°C | ±40V | $R_L$ = 500Ω | 34 | | V |
| 6 | Output Voltage, $I_O$ = 4A | $V_O$ | −55°C | ±30V | $R_L$ = 6Ω | 24 | | V |
| 6 | Stability/Noise | $E_N$ | −55°C | ±34V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 6 | Slew Rate | SR | −55°C | ±34V | $R_L$ = 500Ω | 1.0 | 10 | V/μs |
| 6 | Open Loop Gain | $A_{OL}$ | −55°C | ±34V | $R_L$ = 500Ω, f = 10Hz | 94 | | db |
| 6 | Common-mode Rejection | CMR | −55°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 70 | | db |
| 5 | Output Voltage, $I_O$ = 8A | $V_O$ | 125°C | ±16V | $R_L$ = 1Ω | 8 | | V |
| 5 | Output Voltage, $I_O$ = 68mA | $V_O$ | 125°C | ±40V | $R_L$ = 500Ω | 34 | | V |
| 5 | Output Voltage, $I_O$ = 4A | $V_O$ | 125°C | ±30V | $R_L$ = 6Ω | 24 | | V |
| 5 | Stability/Noise | $E_N$ | 125°C | ±34V | $R_L$ = 500Ω, G = 1, $C_L$ = 1.5nF | | 1 | mV |
| 5 | Slew Rate | SR | 125°C | ±34V | $R_L$ = 500Ω | 1.0 | 10 | V/μs |
| 5 | Open Loop Gain | $A_{OL}$ | 125°C | ±34V | $R_L$ = 500Ω, f = 10Hz | 94 | | db |
| 5 | Common-mode Rejection | CMR | 125°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 70 | | db |

## BURN IN CIRCUIT:



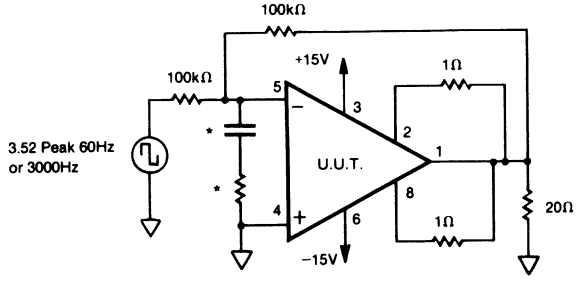

Internal power dissipation is approximately 2.1W at case temperature = 125°C.

*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

## TABLE 4 – GROUP A INSPECTION

| SG | PARAMETER | SYMBOL | TEMP | PWR | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| 1 | Quiescent Current | $I_Q$ | 25°C | ±32V | $V_{IN}$ = 0, G = 100 | | 10 | mA |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±6 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±10.4 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±45V | $V_{IN}$ = 0, G = 100 | | ±8.6 | mV |
| 1 | Input Bias Current, +IN | $+I_B$ | 25°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±30 | nA |
| 1 | Input Bias Current, −IN | $-I_B$ | 25°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±30 | nA |
| 1 | Input Offset Current | $I_{OS}$ | 25°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±30 | nA |
| 3 | Quiescent Current | $I_Q$ | −55°C | ±32V | $V_{IN}$ = 0, G = 100 | | 10 | mA |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±11.2 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±15.6 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±45V | $V_{IN}$ = 0, G = 100 | | ±13.8 | mV |
| 3 | Input Bias Current, +IN | $+I_B$ | −55°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±62 | nA |
| 3 | Input Bias Current, −IN | $-I_B$ | −55°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±62 | nA |
| 3 | Input Offset Current | $I_{OS}$ | −55°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±62 | nA |
| 2 | Quiescent Current | $I_Q$ | 125°C | ±32V | $V_{IN}$ = 0, G = 100 | | 15 | mA |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±12.5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±16.9 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±45V | $V_{IN}$ = 0, G = 100 | | ±15.1 | mV |
| 2 | Input Bias Current, +IN | $+I_B$ | 125°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±70 | nA |
| 2 | Input Bias Current, −IN | $-I_B$ | 125°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±70 | nA |
| 2 | Input Offset Current | $I_{OS}$ | 125°C | ±32V | $V_{IN}$ = 0, G = 100 | | ±70 | nA |
| 4 | Output Voltage, $I_O$ = 10A | $V_O$ | 25°C | ±17V | $R_L$ = 1Ω | 10 | | V |
| 4 | Output Voltage, $I_O$ = 80mA | $V_O$ | 25°C | ±45V | $R_L$ = 500Ω | 40 | | V |
| 4 | Output Voltage, $I_O$ = 4A | $V_O$ | 25°C | ±30V | $R_L$ = 6Ω | 24 | | V |
| 4 | Current Limits | $I_{CL}$ | 25°C | ±15V | $R_L$ = 1Ω, $R_{CL}$ = .1Ω | 5 | 7.9 | A |
| 4 | Stability/Noise | $E_N$ | 25°C | ±32V | $R_L$ = 500Ω, G = 1, $C_L$ = 10nF | | 1 | mV |
| 4 | Slew Rate | SR | 25°C | ±32V | $R_L$ = 500Ω | 1 | 10 | V/μs |
| 4 | Open Loop Gain | $A_{OL}$ | 25°C | ±32V | $R_L$ = 500Ω, f = 10Hz | 96 | | db |
| 4 | Common-mode Rejection | CMR | 25°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 74 | | db |
| 6 | Output Voltage, $I_O$ = 10A | $V_O$ | −55°C | ±17V | $R_L$ = 1Ω | 10 | | V |
| 6 | Output Voltage, $I_O$ = 80mA | $V_O$ | −55°C | ±45V | $R_L$ = 500Ω | 40 | | V |
| 6 | Output Voltage, $I_O$ = 4A | $V_O$ | −55°C | ±30V | $R_L$ = 6Ω | 24 | | V |
| 6 | Stability/Noise | $E_N$ | −55°C | ±32V | $R_L$ = 500Ω, G = 1, $C_L$ = 10nF | | 1 | mV |
| 6 | Slew Rate | SR | −55°C | ±32V | $R_L$ = 500Ω | 1 | 10 | V/μs |
| 6 | Open Loop Gain | $A_{OL}$ | −55°C | ±32V | $R_L$ = 500Ω, f = 10Hz | 96 | | db |
| 6 | Common-mode Rejection | CMR | −55°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 74 | | db |
| 5 | Output Voltage, $I_O$ = 8A | $V_O$ | 125°C | ±15V | $R_L$ = 1Ω | 8 | | V |
| 5 | Output Voltage, $I_O$ = 80mA | $V_O$ | 125°C | ±45V | $R_L$ = 500Ω | 40 | | V |
| 5 | Output Voltage, $I_O$ = 4A | $V_O$ | 125°C | ±30V | $R_L$ = 6Ω | 24 | | V |
| 5 | Stability/Noise | $E_N$ | 125°C | ±32V | $R_L$ = 500Ω, G = 1, $C_L$ = 10nF | | 1 | mV |
| 5 | Slew Rate | SR | 125°C | ±32V | $R_L$ = 500Ω | 1 | 10 | V/μs |
| 5 | Open Loop Gain | $A_{OL}$ | 125°C | ±32V | $R_L$ = 500Ω, f = 10Hz | 96 | | db |
| 5 | Common-mode Rejection | CMR | 125°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 74 | | db |

**BURN IN CIRCUIT:**



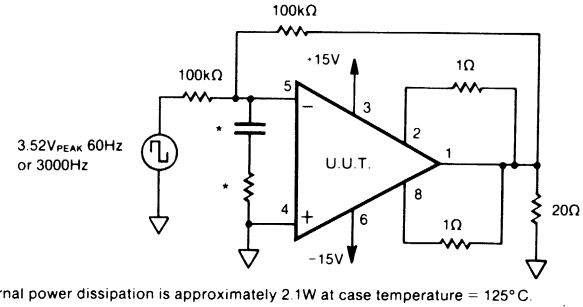

Internal power dissipation is approximately 2.1W at case temperature = 125°C.

*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

## TABLE 4 – GROUP A INSPECTION

| SG | PARAMETER | SYMBOL | TEMP | PWR | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| 1 | Quiescent Current | $I_Q$ | 25°C | ±28V | $V_{IN}$ = 0, G = 100 | | 5 | mA |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±10 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±17.2 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±30V | $V_{IN}$ = 0, G = 100 | | ±10.8 | mV |
| 1 | Input Bias Current, +IN | $+I_B$ | 25°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±40 | nA |
| 1 | Input Bias Current, −IN | $-I_B$ | 25°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±40 | nA |
| 1 | Input Offset Current | $I_{OS}$ | 25°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±10 | nA |
| 3 | Quiescent Current | $I_Q$ | −55°C | ±28V | $V_{IN}$ = 0, G = 100 | | 5 | mA |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±15.2 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±22.4 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±30V | $V_{IN}$ = 0, G = 100 | | ±16 | mV |
| 3 | Input Bias Current, +IN | $+I_B$ | −55°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±72 | nA |
| 3 | Input Bias Current, −IN | $-I_B$ | −55°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±72 | nA |
| 3 | Input Offset Current | $I_{OS}$ | −55°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±26 | nA |
| 2 | Quiescent Current | $I_Q$ | 125°C | ±28V | $V_{IN}$ = 0, G = 100 | | 7 | mA |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±16.5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±10V | $V_{IN}$ = 0, G = 100 | | ±23.7 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±30V | $V_{IN}$ = 0, G = 100 | | ±17.3 | mV |
| 2 | Input Bias Current, +IN | $+I_B$ | 125°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±80 | nA |
| 2 | Input Bias Current, −IN | $-I_B$ | 125°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±80 | nA |
| 2 | Input Offset Current | $I_{OS}$ | 125°C | ±28V | $V_{IN}$ = 0, G = 100 | | ±30 | nA |
| 4 | Output Voltage, $I_O$ = 5A | $V_O$ | 25°C | ±18.3V | $R_L$ = 2.07Ω | 10.3 | | V |
| 4 | Output Voltage, $I_O$ = 50mA | $V_O$ | 25°C | ±30V | $R_L$ = 500Ω | 25 | | V |
| 4 | Output Voltage, $I_O$ = 2A | $V_O$ | 25°C | ±30V | $R_L$ = 12Ω | 24 | | V |
| 4 | Current Limits | $I_{CL}$ | 25°C | ±16V | $R_L$ = 2.07Ω, $R_{CL}$ = .2Ω | 2.6 | 3.9 | A |
| 4 | Stability/Noise | $E_N$ | 25°C | ±28V | $R_L$ = 500Ω, G = 1, $C_L$ = 10nF | | 1 | mV |
| 4 | Slew Rate | SR | 25°C | ±28V | $R_L$ = 500Ω | 1 | 10 | V/μs |
| 4 | Open Loop Gain | $A_{OL}$ | 25°C | ±28V | $R_L$ = 500Ω, f = 10Hz | 91 | | db |
| 4 | Common-mode Rejection | CMR | 25°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 70 | | db |
| 6 | Output Voltage, $I_O$ = 5A | $V_O$ | −55°C | ±18.3V | $R_L$ = 2.07Ω | 10.3 | | V |
| 6 | Output Voltage, $I_O$ = 50mA | $V_O$ | −55°C | ±30V | $R_L$ = 500Ω | 25 | | V |
| 6 | Output Voltage, $I_O$ = 2A | $V_O$ | −55°C | ±30V | $R_L$ = 12Ω | 24 | | V |
| 6 | Stability/Noise | $E_N$ | −55°C | ±28V | $R_L$ = 500Ω, G = 1, $C_L$ = 10nF | | 1 | mV |
| 6 | Slew Rate | SR | −55°C | ±28V | $R_L$ = 500Ω | 1 | 10 | V/μs |
| 6 | Open Loop Gain | $A_{OL}$ | −55°C | ±28V | $R_L$ = 500Ω, f = 10Hz | 91 | | db |
| 6 | Common-mode Rejection | CMR | −55°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 70 | | db |
| 5 | Output Voltage, $I_O$ = 3A | $V_O$ | 125°C | ±11.3V | $R_L$ = 2.07Ω | 6.3 | | V |
| 5 | Output Voltage, $I_O$ = 50mA | $V_O$ | 125°C | ±30V | $R_L$ = 500Ω | 25 | | V |
| 5 | Output Voltage, $I_O$ = 2A | $V_O$ | 125°C | ±30V | $R_L$ = 12Ω | 24 | | V |
| 5 | Stability/Noise | $E_N$ | 125°C | ±28V | $R_L$ = 500Ω, G = 1, $C_L$ = 10nF | | 1 | mV |
| 5 | Slew Rate | SR | 125°C | ±28V | $R_L$ = 500Ω | 1 | 10 | V/μs |
| 5 | Open Loop Gain | $A_{OL}$ | 125°C | ±28V | $R_L$ = 500Ω, f = 10Hz | 91 | | db |
| 5 | Common-mode Rejection | CMR | 125°C | ±15V | $R_L$ = 500Ω, f = DC, $V_{CM}$ = ±9V | 70 | | db |

## BURN IN CIRCUIT:



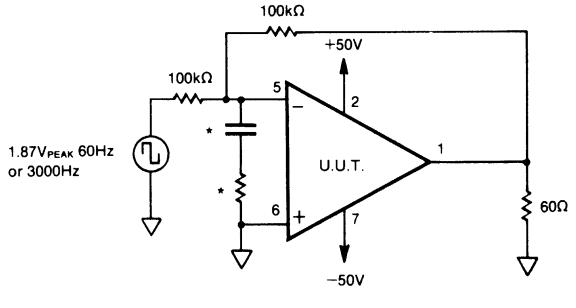

Internal power dissipation is approximately 2.1W at case temperature = 125°C.

*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

## TABLE 4—GROUP A INSPECTION

| SG | PARAMETER | SYMBOL | TEMP | PWR | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| 1 | Quiescent Current | $I_Q$ | 25°C | ±150V | $V_{IN}$ = 0, G = 100 | | 8.5 | mA |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±150V | $V_{IN}$ = 0, G = 100 | | 3 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±15V | $V_{IN}$ = 0, G = 100 | | 5.7 | mV |
| 1 | Input Bias Current, +IN | $+I_B$ | 25°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 1 | Input Bias Current, −IN | $-I_B$ | 25°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 1 | Input Offset Current | $I_{OS}$ | 25°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Quiescent Current | $I_Q$ | −55°C | ±150V | $V_{IN}$ = 0, G = 100 | | 10 | mA |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±150V | $V_{IN}$ = 0, G = 100 | | 5 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±15V | $V_{IN}$ = 0, G = 100 | | 7.7 | mV |
| 3 | Input Bias Current, +IN | $+I_B$ | −55°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Input Bias Current, −IN | $-I_B$ | −55°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Input Offset Current | $I_{OS}$ | −55°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 2 | Quiescent Current | $I_Q$ | 125°C | ±150V | $V_{IN}$ = 0, G = 100 | | 10 | mA |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±150V | $V_{IN}$ = 0, G = 100 | | 5.5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±15V | $V_{IN}$ = 0, G = 100 | | 8.2 | mV |
| 2 | Input Bias Current, +IN | $+I_B$ | 125°C | ±150V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Bias Current, −IN | $-I_B$ | 125°C | ±150V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Offset Current | $I_{OS}$ | 125°C | ±150V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 4 | Output Voltage, $I_O$ = 75mA | $V_O$ | 25°C | ±85V | $R_L$ = 1K | 75 | | V |
| 4 | Output Voltage, $I_O$ = 29mA | $V_O$ | 25°C | ±150V | $R_L$ = 5K | 145 | | V |
| 4 | Current Limits | $I_{CL}$ | 25°C | ±30V | $R_L$ = 100Ω | 75 | 125 | mA |
| 4 | Stability/Noise | $E_N$ | 25°C | ±150V | $R_L$ = 5K, G = 1, $C_L$ = 10nF | | 1 | mV |
| 4 | Slew Rate | SR | 25°C | ±150V | $R_L$ = 5K | 20 | 60 | V/μs |
| 4 | Open Loop Gain | $A_{OL}$ | 25°C | ±150V | $R_L$ = 5K, f = 10Hz | 96 | | db |
| 4 | Common-mode Rejection | CMR | 25°C | ±32.5V | $R_L$ = 5K, f = DC, $V_{CM}$ = ±22.5V | 90 | | db |
| 6 | Output Voltage, $I_O$ = 40mA | $V_O$ | −55°C | ±45V | $R_L$ = 1K | 40 | | V |
| 6 | Output Voltage, $I_O$ = 29mA | $V_O$ | −55°C | ±150V | $R_L$ = 5K | 145 | | V |
| 6 | Stability/Noise | $E_N$ | −55°C | ±150V | $R_L$ = 5K, G = 1, $C_L$ = 10nF | | 1 | mV |
| 6 | Slew Rate | SR | −55°C | ±150V | $R_L$ = 5K | 20 | 60 | V/μs |
| 6 | Open Loop Gain | $A_{OL}$ | −55°C | ±150V | $R_L$ = 5K, f = 10Hz | 96 | | db |
| 6 | Common-mode Rejection | CMR | −55°C | ±32.5V | $R_L$ = 5K, f = DC, $V_{CM}$ = ±22.5V | 90 | | db |
| 5 | Output Voltage, $I_O$ = 40mA | $V_O$ | 125°C | ±45V | $R_L$ = 1K | 40 | | V |
| 5 | Output Voltage, $I_O$ = 29mA | $V_O$ | 125°C | ±150V | $R_L$ = 5K | 145 | | V |
| 5 | Stability/Noise | $E_N$ | 125°C | ±150V | $R_L$ = 5K, G = 1, $C_L$ = 10nF | | 1 | mV |
| 5 | Slew Rate | SR | 125°C | ±150V | $R_L$ = 5K | 20 | 60 | V/μs |
| 5 | Open Loop Gain | $A_{OL}$ | 125°C | ±150V | $R_L$ = 5K, f = 10Hz | 96 | | db |
| 5 | Common-mode Rejection | CMR | 125°C | ±32.5V | $R_L$ = 5K, f = DC, $V_{CM}$ = ±22.5V | 90 | | db |

**BURN IN CIRCUIT:**



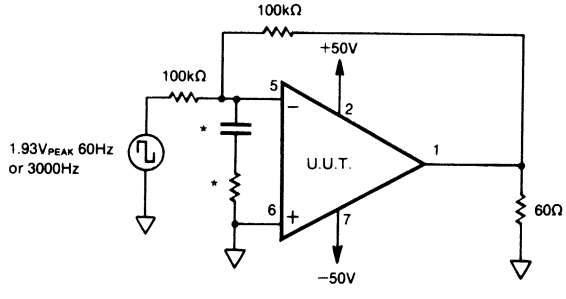

Internal power dissipation is approximately 2.1W at case temperature = 125°C.

*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

## TABLE 4 — GROUP A INSPECTION

| SG | PARAMETER | SYMBOL | TEMP | PWR | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| 1 | Quiescent Current | $I_Q$ | 25°C | ±150V | $V_{IN}$ = 0, G = 100 | | 7.5 | mA |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±150V | $V_{IN}$ = 0, G = 100 | | 3 | mV |
| 1 | Input Offset Voltage | $V_{OS}$ | 25°C | ±15V | $V_{IN}$ = 0, G = 100 | | 5.7 | mV |
| 1 | Input Bias Current, +IN | $+I_B$ | 25°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 1 | Input Bias Current, −IN | $-I_B$ | 25°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 1 | Input Offset Current | $I_{OS}$ | 25°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Quiescent Current | $I_Q$ | −55°C | ±150V | $V_{IN}$ = 0, G = 100 | | 9.5 | mA |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±150V | $V_{IN}$ = 0, G = 100 | | 5 | mV |
| 3 | Input Offset Voltage | $V_{OS}$ | −55°C | ±15V | $V_{IN}$ = 0, G = 100 | | 7.7 | mV |
| 3 | Input Bias Current, +IN | $+I_B$ | −55°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Input Bias Current, −IN | $-I_B$ | −55°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 3 | Input Offset Current | $I_{OS}$ | −55°C | ±150V | $V_{IN}$ = 0, G = 100 | | 50 | pA |
| 2 | Quiescent Current | $I_Q$ | 125°C | ±150V | $V_{IN}$ = 0, G = 100 | | 9.5 | mA |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±150V | $V_{IN}$ = 0, G = 100 | | 5.5 | mV |
| 2 | Input Offset Voltage | $V_{OS}$ | 125°C | ±15V | $V_{IN}$ = 0, G = 100 | | 8.2 | mV |
| 2 | Input Bias Current, +IN | $+I_B$ | 125°C | ±150V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Bias Current, −IN | $-I_B$ | 125°C | ±150V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 2 | Input Offset Current | $I_{OS}$ | 125°C | ±150V | $V_{IN}$ = 0, G = 100 | | 10 | nA |
| 4 | Output Voltage, $I_O$ = 40mA | $V_O$ | 25°C | ±47V | $R_L$ = 1K | 40 | | V |
| 4 | Output Voltage, $I_O$ = 28.6mA | $V_O$ | 25°C | ±150V | $R_L$ = 5K | 143 | | V |
| 4 | Output Voltage, $I_O$ = 15mA | $V_O$ | 25°C | ±80V | $R_L$ = 5K | 75 | | V |
| 4 | Current Limits | $I_{CL}$ | 25°C | ±20V | $R_L$ = 100Ω | 36 | 70 | mA |
| 4 | Stability/Noise | $E_N$ | 25°C | ±150V | $R_L$ = 5K, G = 1, $C_L$ = 10nF | | 1 | mV |
| 4 | Slew Rate | SR | 25°C | ±150V | $R_L$ = 5K, $C_C$ = 50pF | 100 | 600 | V/μs |
| 4 | Open Loop Gain | $A_{OL}$ | 25°C | ±150V | $R_L$ = 5K, f = 10Hz | 100 | | db |
| 4 | Common-mode Rejection | CMR | 25°C | ±32.5V | $R_L$ = 5K, f = DC, $V_{CM}$ = ±22.5V | 90 | | db |
| 6 | Output Voltage, $I_O$ = 40mA | $V_O$ | −55°C | ±47V | $R_L$ = 1K | 40 | | V |
| 6 | Output Voltage, $I_O$ = 28.6mA | $V_O$ | −55°C | ±150V | $R_L$ = 5K | 143 | | V |
| 6 | Output Voltage, $I_O$ = 15mA | $V_O$ | −55°C | ±80V | $R_L$ = 5K | 75 | | V |
| 6 | Stability/Noise | $E_N$ | −55°C | ±150V | $R_L$ = 5K, G = 1, $C_L$ = 10nF | | 1 | mV |
| 6 | Slew Rate | SR | −55°C | ±150V | $R_L$ = 5K, $C_C$ = 50pF | 100 | 600 | V/μs |
| 6 | Open Loop Gain | $A_{OL}$ | −55°C | ±150V | $R_L$ = 5K, f = 10Hz | 100 | | db |
| 6 | Common-mode Rejection | CMR | −55°C | ±32.5V | $R_L$ = 5K, f = DC, $V_{CM}$ = ±22.5V | 90 | | db |
| 5 | Output Voltage, $I_O$ = 30mA | $V_O$ | 125°C | ±37V | $R_L$ = 1K | 30 | | V |
| 5 | Output Voltage, $I_O$ = 28.6mA | $V_O$ | 125°C | ±150V | $R_L$ = 5K | 143 | | V |
| 5 | Output Voltage, $I_O$ = 15mA | $V_O$ | 125°C | ±80V | $R_L$ = 5K | 75 | | V |
| 5 | Stability/Noise | $E_N$ | 125°C | ±150V | $R_L$ = 5K, G = 1, $C_L$ = 10nF | | 1 | mV |
| 5 | Slew Rate | SR | 125°C | ±150V | $R_L$ = 5K, $C_C$ = 50pF | 100 | 600 | V/μs |
| 5 | Open Loop Gain | $A_{OL}$ | 125°C | ±150V | $R_L$ = 5K, f = 10Hz | 100 | | db |
| 5 | Common-mode Rejection | CMR | 125°C | ±32.5V | $R_L$ = 5K, f = DC, $V_{CM}$ = ±22.5V | 90 | | db |

## BURN IN CIRCUIT:

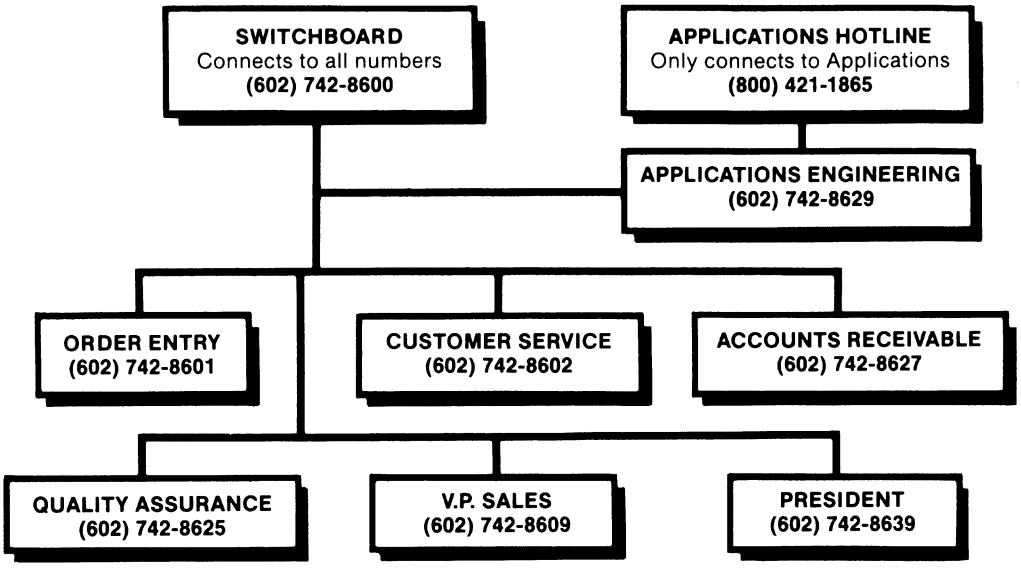



Internal power dissipation is approximately 2.1W at case temperature = 125°C.

*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

# ACCESS DIRECTORY

## TELEX: 170631



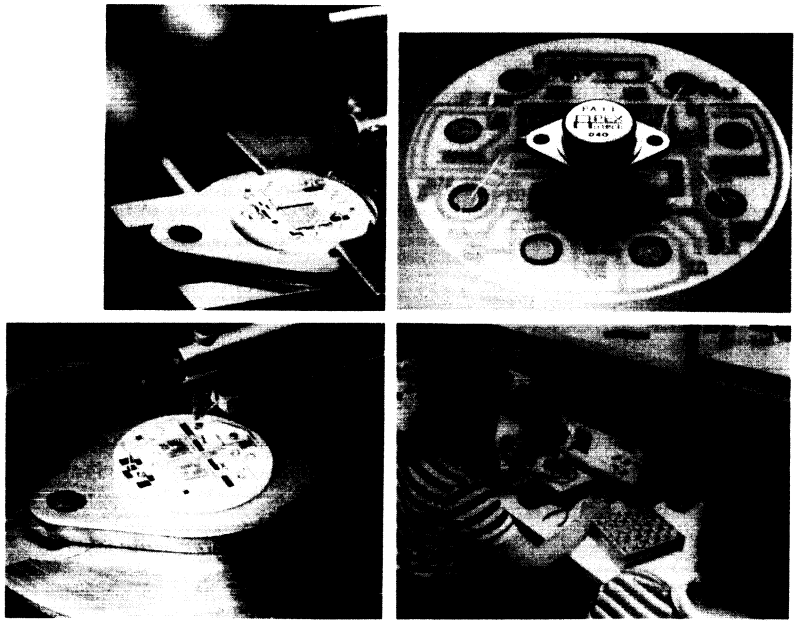

## STANDARD HOURS:

| | MOUNTAIN STANDARD TIME | GREENWICH MEAN TIME |
|---|---|---|
| SWITCH BOARD: | 8:00 AM to 4:30 PM | 15:00 to 23:30 |
| ORDER ENTRY: | 7:00 AM to 5:00 PM | 14:00 to 24:00 |
| OTHER: | 8:00 AM to 4:00 PM | 15:00 to 23:00 |

**APEX MICROTECHNOLOGY CORP. (Domestic)**
**APEX F.S.C. INC. (Export)**
5980 N. SHANNON ROAD, TUCSON, AZ 85741, USA

# •ACCESSORIES AND PACKAGE DATA

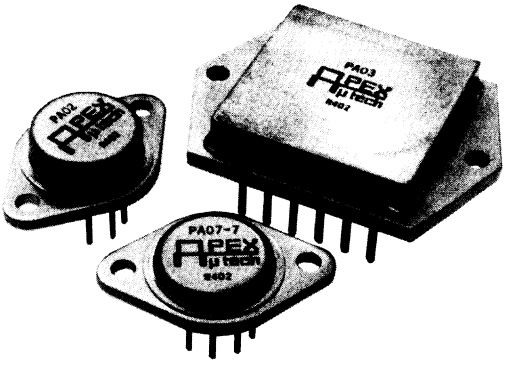
***To ease the hardware design . . .***



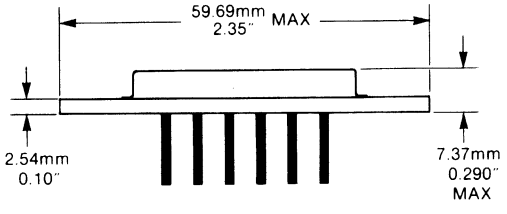
# PACKAGE OUTLINES
## POWER OPERATIONAL AMPLIFIERS

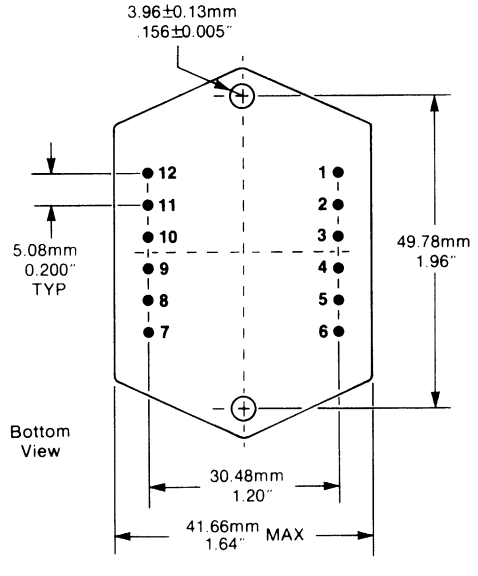
## DESCRIPTION

Power device packages must not only provide a sealed environment for the product, but also withstand the mechanical rigors of mounting and thermal cycling while providing a low thermal resistance from active components to the heat sink. The industry standard 8 pin TO-3 package does an outstanding job of housing many Apex power products. The Apex high power package was developed to provide power levels well above the TO-3 package. The copper platform improves thermal conductivity by an order of magnitude over steel. It also provides a much better coefficient of expansion match to aluminum heat sinks and insure long term performance.



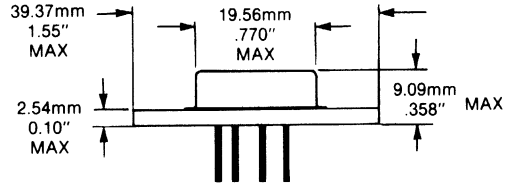

## HIGH POWER

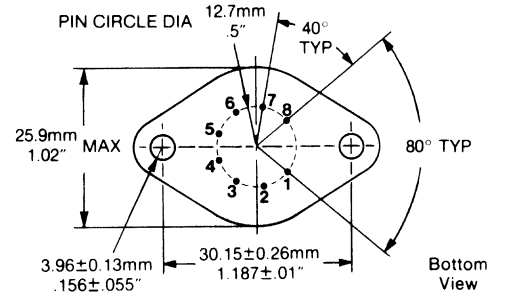



| | |
|---|---|
| PIN DIAMETER: | 1.52mm or 0.06" |
| PIN LENGTH: | 10.2mm or 0.40" MIN |
| PIN MATERIAL: | Gold plated alloy 52, solderable |
| PLATFORM MATERIAL: | Gold plated copper |
| CAP MATERIAL: | Nickel plated steel |
| SEAL: | Hermetic, soldered |
| ISOLATION: | 300VDC any pin to case |
| WEIGHT: | 45 grams |
| CAGE JACKS: | APEX PN: MS04 |
| HEATSINK: | APEX PN: HS06 |

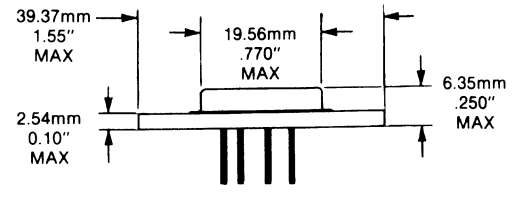
## STANDARD 8 PIN TO-3



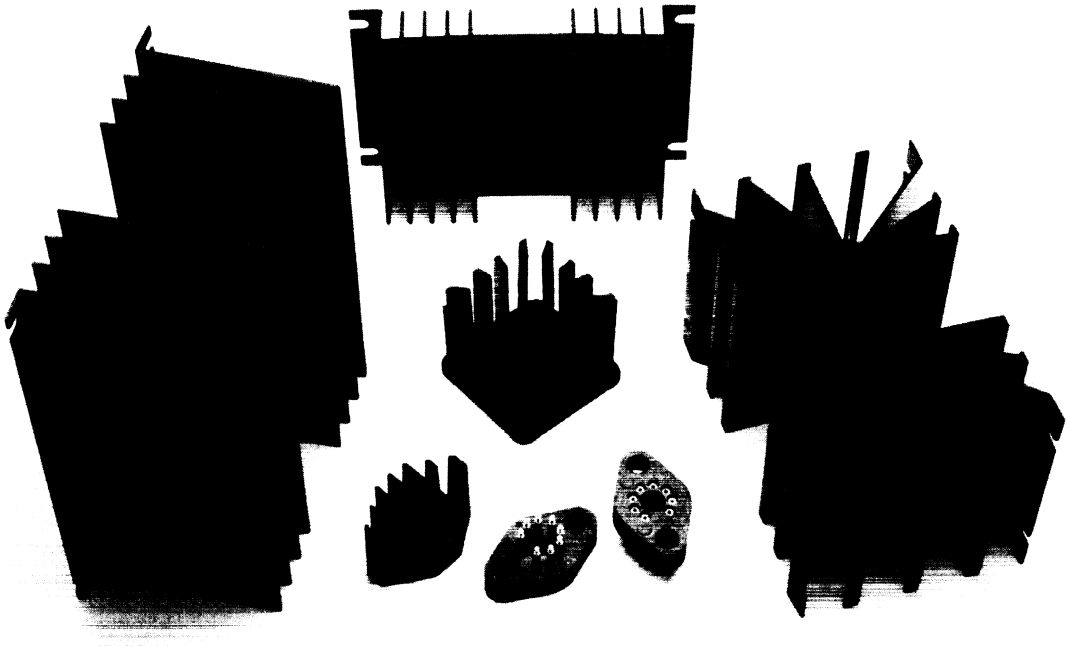




| | |
|---|---|
| PIN DIAMETER: | 1.01mm or 0.04" |
| PIN LENGTH: | 10.2mm or 0.40" MIN |
| PIN MATERIAL, STD: | Nickel plated alloy 52, solderable |
| PIN MATERIAL, MIL: | Gold plated alloy 52, solderable |
| PACKAGE: | Hermetic, nickel plated steel |
| WEIGHT: | 15 grams |
| ISOLATION: | 300VDC any pin to case |
| SOCKETS: | APEX PNs: MS03 |
| CAGE JACKS: | APEX PN: MS02 (set of 8) |
| HEATSINKS: | APEX PNs: HS01 thru HS05 |

## SPECIAL LOW PROFILE TO-3



# HEATSINKS MATING SOCKETS



## HEATSINKS

A wide spectrum of applications can be satisfied with the heatsinks stocked as accessories for APEX power amplifiers. All are made of aluminum and are black anodized to provide high levels of both conduction and radiation. HS01 clamps over the TO-3 case using virtually no additional space on a printed circuit board. HS02 is suitable for chassis or printed circuit mounting. HS03 thru HS05 are designed for chassis mounting. All chassis mountable heatsinks are pre-drilled for the 8 pin TO-3 hole pattern. In large volume these heatsinks may be procured from AAVID Engineering Inc. Conservative calculations are recommended for prototype work while performance graphs are included to enable optimisation for production runs. Due to calculation complexity of thermal circuits and of power dissipation levels where reactive loads are driven, it is often helpful to utilize temperature measurements after the electrical design has been completed.

| APEX PN | RATING 1 | RATING 2 | RATING 3 | AVVID PN |
|---|---|---|---|---|
| HS01 | 11.6 | 6.0 | 4.2 | 5423B |
| HS02 | 4.5 | 3.2 | 2.5 | 5680B-0150-15 |
| HS03 | 1.7 | 1.4 | 1.0 | 6050-3B-15 |
| HS04 | .95 | .57 | .44 | 60650-3B-15 |
| HS05 | .85 | .7 | .53 | 6055-5.5B-15 |

Ratings are all thermal resistances from amplifier mounting surface to ambient expressed as °C/W. Rating 1 is for an unobstructed mounting of optimum orientation. Rating 2 pertains to forced air at a velocity of 100 FPM and Rating 3 is for 200 FPM.

## SOCKETS

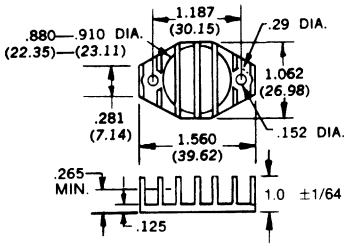
The MS03 Mating Socket is suitable for chassis or heatsink mounting of power op amps. It has a polyethersulfone body that surrounds the eight tin plated brass receptacles holding the gold plated beryllium copper contacts. The contacts are recessed with tapered openings to help align pins as an amplifier is inserted. The blind contacts have an extra deep cavity to allow flush seating of amplifiers with ½" length pins. Mounting holes are counter sunk at the top surface for #6 screws to facilitate chassis mounting. A hexagonal recess on the bottom along with the flat upper surface makes these sockets ideal for heatsink mounting.

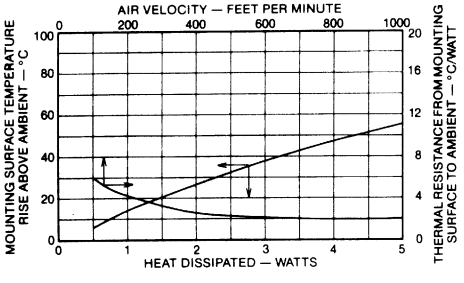
## CAGE JACKS

The MS02 is a set of 8 cage jacks recommended for printed circuit mounting of power op amps. These jacks consist of 2 pieces, a copper body and beryllium copper spring. Both are gold plated for reliable contact and easy wettability by solder. The body diameter is .090" and the length is .221". A #48 drill is recommended for the mounting holes in glass epoxy boards. The bottom can be knocked out with special tools (or even a pin punch) to accommodate long pins. These Cage Jacks are made by Cambion, PN: 450-3716-01-03-00.

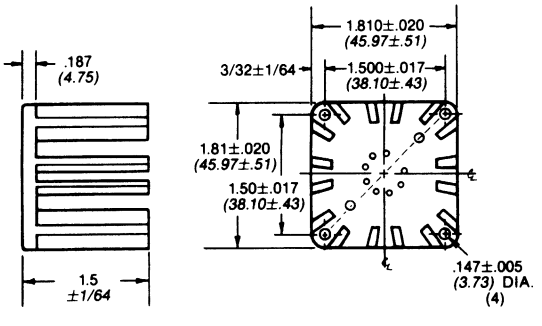
# HEATSINKS

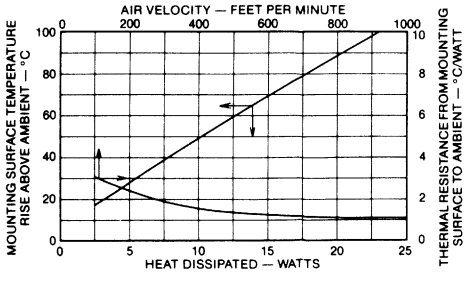
## HS01



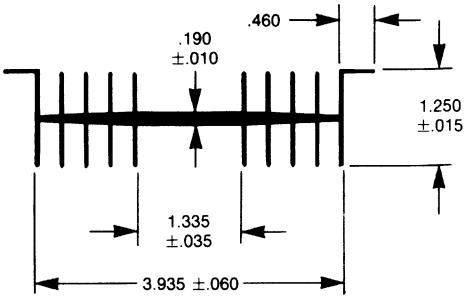



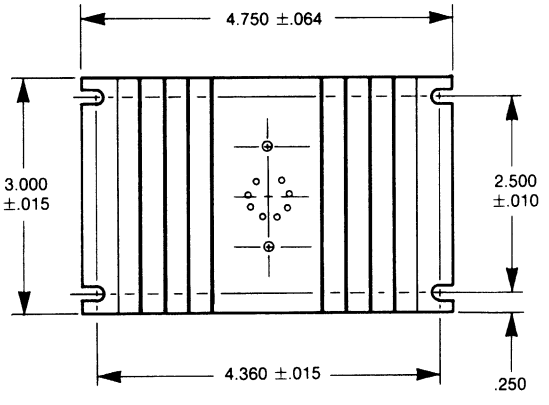

## HS02



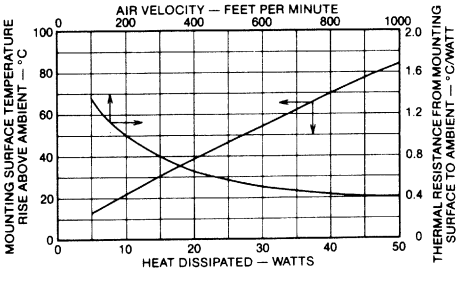




## HS03



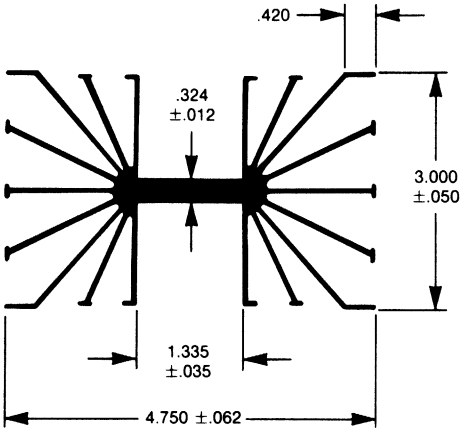



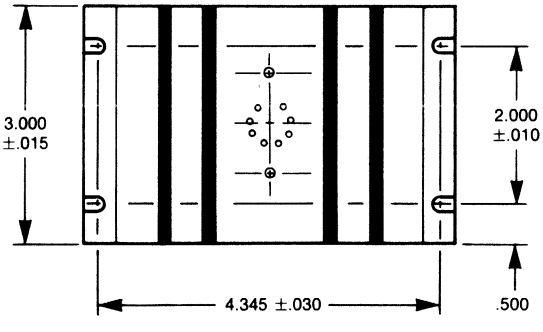

Mounting Holes (4): .190 ±.006 DIA



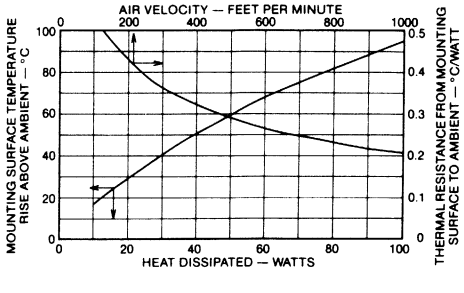
# HEATSINKS

## HS04

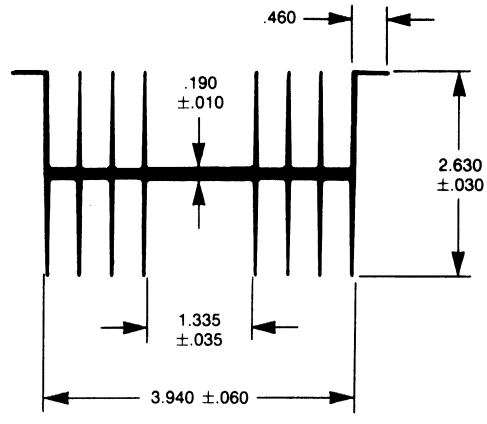


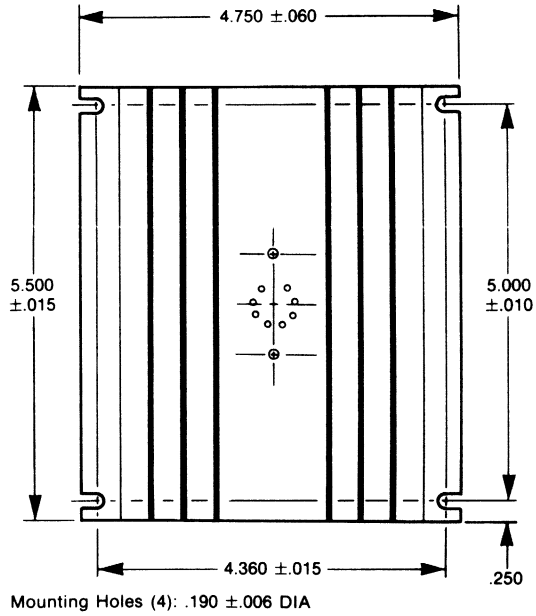




Mounting Holes (8): .190 ±.006 DIA

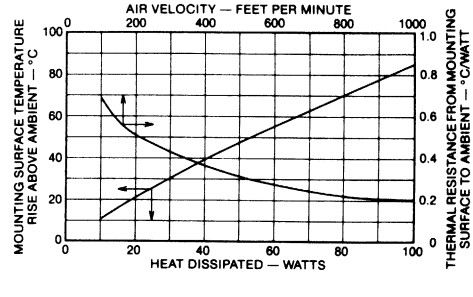



## HS05



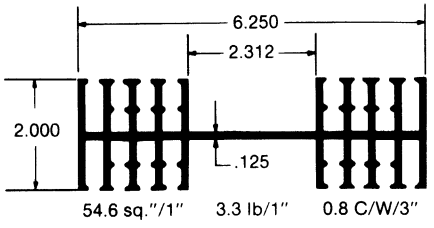



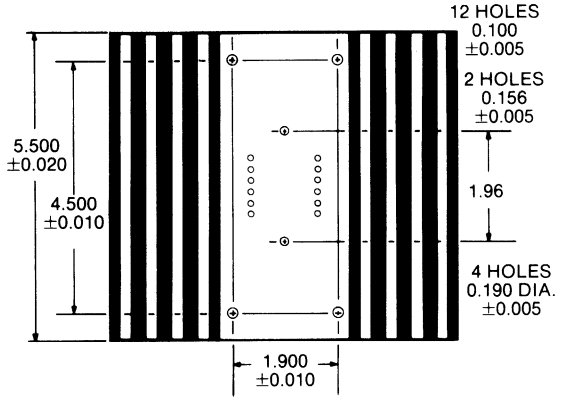

Mounting Holes (4): .190 ±.006 DIA



# HEATSINKS

## HS06



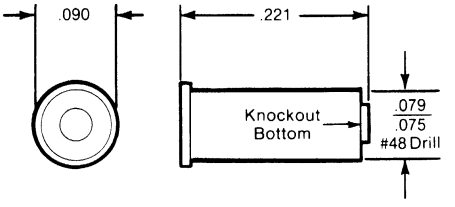




STANDARD COMMERCIAL EXTRUSION TOLERANCES APPLY

MATERIAL ALUMINUM ALLOY
FINISH: BLACK ANODIZE
THERMAL RESISTANCE: ≅ .6°C/W
AAVID P/N: A-002-141-39

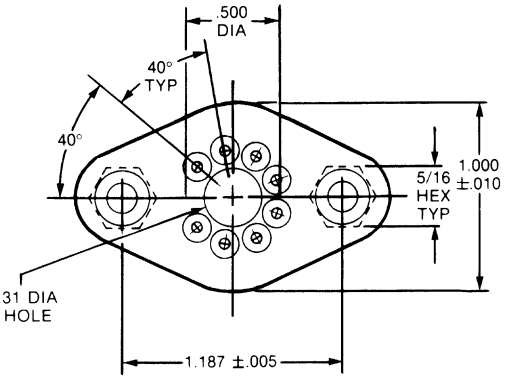
# SOCKETS

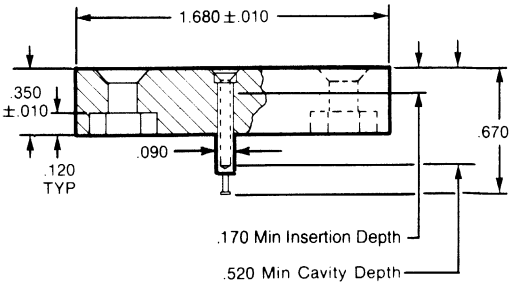
## MS02




Minimum Insertion Depth: .10
Knockout Tools
Tip: 435-3935-01-00-00
Impact Tool: 435-3101-00-00
1:1 Layout Template is Available
Cambion PN: 450-3716-01-03

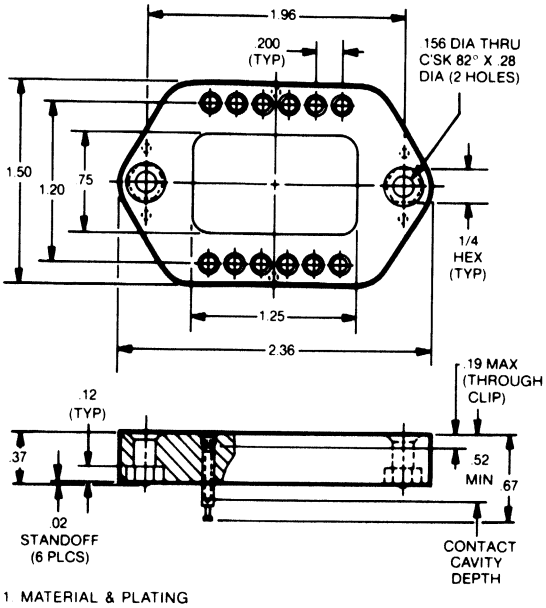
## MS03




Mounting Holes (2): .160 Thru, CSK 82° x .290
Material: Polyethersulfone or equivalent.

## MS05

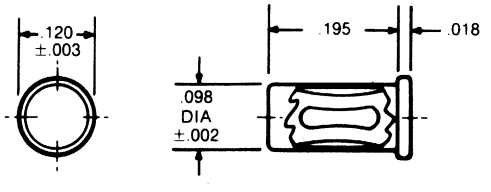



1 MATERIAL & PLATING
SOCKET BODY: POLYESTER, GLASS FILLED, 94 $V_O$ RATING
COLOR - GREEN
CONTACTS: BODY-BRASS, .002 TIN OVER .0001 NICKEL PLATE
CLIP-$B_EC_U$ .00003 GOLD OVER .00005 NICKEL PLATE
TEMPERATURE RATING: 150°C (CONTINUOUS)

## CAGE JACKS

## MS04

### .060 DIA. PINS




HOLE DEPTH: .200 MINIMUM
MATERIAL: BODY: BRASS
SPRING: BERYLLIUM COPPER
FINISH: BODY: .00002 SOFT GOLD OVER .0002 COPPER
SPRING: .0005 HARD GOLD OVER .0002 COPPER
RECOMMENDED MOUNTING HOLE: .102 ±.002 DIA. (#38 DRILL)
CAMBION PN: 450-3326-01-03-00

## TECHNICAL NOTES

The cases of all APEX power op amps are isolated from the internal circuitry to provide low thermal resistance and allow flexibility in mounting. To achieve optimum performance, these power op amps should be mounted directly to grounded heat-sinks without insulating washers.

The addition of an insulating washer, as required with some products having a non-isolated case, adds resistance to the thermal path. Typical values for both 5.7 mil mica and 2 mil kapton washers are .8°C/W as opposed to .2°C/W without a washer (thermal joint compound used in all cases). For the PA12 in an AC application, inclusion of one of these washers increases the typical thermal resistance from junction to heatsink by 60%. The resulting degradation requires additional cooling capacity or the operating junction temperatures will rise. The first alternative will directly affect the cost of the product and the second the reliability. To illustrate the reliability effect, figure 1 shows the average failure rates of the NPN and PNP output power transistors at varying junction temperatures relative to operation at 25°C. This data was extracted from the base failure rate tables of MIL-HDBK-217C, revision of 1 May 1980.

Isolated cases can also cause problems due to capacitance to the pins and/or internal nodes, especially when the amplifier is to be mounted side by side with hot case components. There are two prime modes of coupling where these capacitances degrade circuit performance or cause oscillations. The first mode arises when the case and/or heatsinks are left totally floating. An unwanted feedback path can be formed between the highly sensitive amplifier input stage and the output with it's large voltage swing. Input impedance, PC layout and mounting technique can influence circuit peformance and produce unpredictable results.

The second mode of coupling arises when the case and heatsink are tied to the chassis (power neutral), which is not an AC ground of the circuit in question. In this case, error signals with reference to the AC ground of the power op amp circuit can introduce noise, distortion or even oscillations. The preferred solution in this case is to isolate the heatsink from the chassis and connect it (and thereby the amplifier case) to the local AC ground. The use of an insulating washer should be considered as a last resort only when the chassis is used for thermal dissipation and cannot be connected to the correct ground.

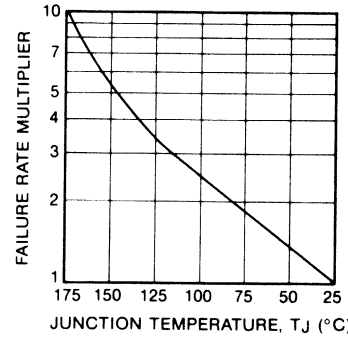



**FIG. 1: MTTF vs TEMPERATURE**

## MECHANICAL RECOMMENDATIONS

1. Use #6 mounting hardware to provide adequate thermal joints and accurate alignment of pins.
2. Include Belville washers to maintain thermal conductance through the life of the product.
3. Torque mounting screws 4 to 7 inch pounds when steel alloy or brass, but limiting to 5.3 inch pounds for aluminum.
4. Use thermal joint compound for all mountings, especially inside the pin circle. (Location of the power transistors where the majority of heat is transferred from case to heatsink.)
5. Do not drill a single hole for all 8 pins or enlarge the pin holes of heatsinks for clearance. The major thermal path is from inside the pin circle to the fins of the heatsink, thus the amount of material between pins will have a substantial effect on circuit performance.

# VENDORS FOR POWER OP AMP ACCESSORIES . . .

*The following list answers the most common requests received on the APEX Applications Hotline. It is by no means a complete list of sources, but can save you valuable time locating your requirements.*

## • CAGE JACKS

CAMBION
445 Concord Ave.
Cambridge, MA 02238
(617) 491-5400

CONCORD
30 Great Jones St.
New York, NY 10012
(212) 777-6571

## • HEATSINKS

AAVID ENGINEERING, INC.
30 Cook Court, Box 400
Laconia, NH 03247
(603) 524-4443

EG&G WAKEFIELD ENGINEERING
60 Audubon Road
Wakefield, MA 01880
(617) 245-5900

INTERNATIONAL ELECTRONIC RESEARCH CORP.
P.O. Box 7704
Burbank, CA 91510-7704
(213) 849-2481

THERMALLOY, INC.
P.O. Box 340839
2021 West Valley View Lane
Dallas, TX 75234-9990
(214) 243-4321

## • LOW VALUE RESISTORS

KELVIN
5919 Noble Avenue
Van Nuys, CA 91411
(213) 782-6662

RCL ELECTRONICS, INC.
195 McGregor St.
Manchester, NH 03102
(603) 627-3831

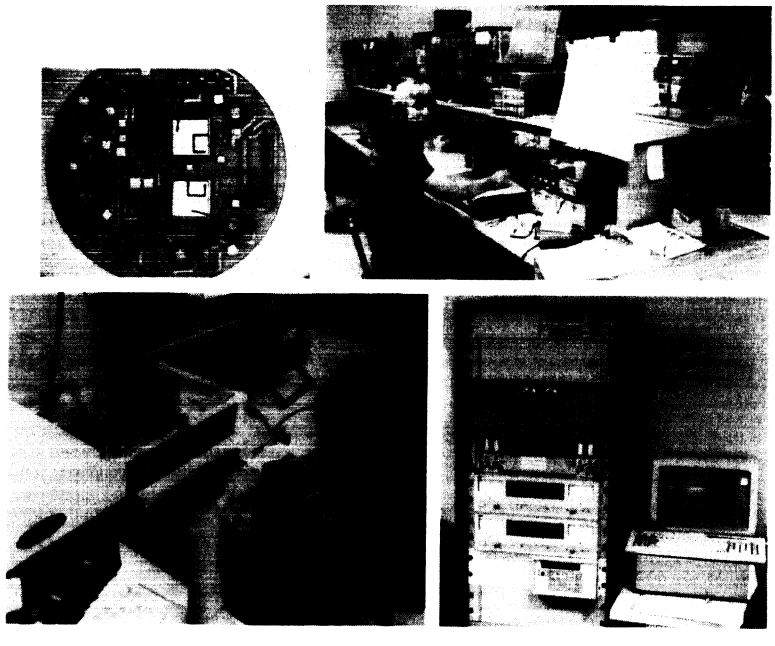
RIEDON DIVISION
M.W. Riedel & Co.
625 Monterey Pass Road
Monterey Park, CA 91754
(213) 283-7694

## • RESISTANCE WIRE

MWS WIRE INDUSTRIES
31200 Cedar Valley Drive
Westlake Village, CA 91362
(818) 991-8553

# •PARAMETER DEFINITIONS AND TEST METHODS

***To achieve the best possible performance . . .***



# PARAMETER DEFINITIONS AND TEST METHODS

1. ***Absolute maximum ratings:***
Absolute maximum ratings are stress levels which may be applied to the amplifier one at a time. The amplifier will not suffer permanent damage, however, proper operation is not implied. Simultaneous application of two or more of these maximum stress levels may induce permanent damage to the amplifier.

2. ***Differential input voltage:***
Differential input voltage is the voltage difference between the two input pins. It will be near zero in any linear (nonsaturated) operating mode. Non-zero voltages arise with very fast rising input waveforms, shorted outputs, overdriven inputs, and other abnormal conditions.

3. ***RTI (Referred to the input):***
All input errors will be seen at the output of the amplifier at an amplitude equal to the input error term times the noninverting gain of the circuit. (Errors are seen from the noninverting input pin, ie. voltage offset will appear at a gain of two at the output in an inverting gain of one circuit.)

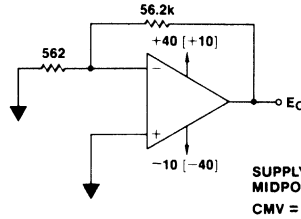
4. ***Loop gain:***
Loop gain is the difference between open loop gain and the gain of the external circuit. This excess gain over the required signal amplification is the key feature of all operational amplifiers that provides a proportional increase in accuracy.

5. ***Typical supply voltage:***
Typical supply voltage is a value which APEX has determined to be the optimum voltage to specify. This value is influenced by both customer input and competitor specifications.

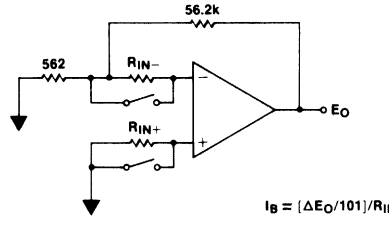
6. ***Common-mode impedance: $Z_{IN}$***
$Z_{IN}$ is the effective impedance from either input to common (ground). Because most op amps do not have ground pins, the specification is often referred to the mid point of the two power pin voltages as in the case of single supplies. Measuring the effect of a known source impedance driving a buffer configuration will yield common-mode input impedance. Low frequency inputs are used to characterize resistive elements and higher frequencies enable measuring capacitive elements of the input impedance. This value is generally very high and can be neglected. Therefore it is usually part of the design characterization data rather than a 100% tested parameter.

7. ***Common-mode voltage: CMV***
CMV is the average (common component) of the two input voltages with respect to the mid point of the two power supply voltages (ground in the case of dual symmetric supplies). Because most op amps do not have ground pins, the parameter is often specified as a minimum voltage difference between the CMV and either supply rail. When operating on a single supply, the CMV specifications of APEX amplifiers do not allow input pin voltages to reach zero or the supply voltage. In any nonsaturated operating mode, both input voltages will be essentially equal.

8. ***Common-mode rejection: CMR***
Common-mode rejection is the ability of the amplifier to reject two equal input signals as they vary from the midpoint of the two supply voltages (ground in the case of dual symmetric supplies).

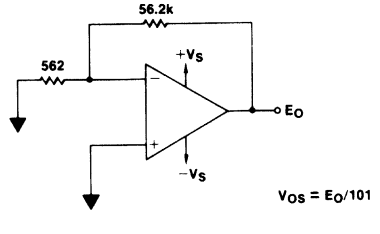



9. ***Input bias current: $I_B$***
$I_B$ is the net current flowing into or out of the amplifier input pins at a zero signal condition. This current results from base currents of bipolar input transistors (sometimes reduced by cancellation networks) or gate leakage of FET input transistors. Measurement techniques require insertion of very large impedances in series with the inputs and converting the resulting output voltage change to a bias current in accordance with Ohm's Law.




10. ***Input offset current: $I_{OS}$***
$I_{OS}$ is the difference between the two bias currents. The offset current rating is generally smaller than the bias current rating which implies that matching impedances for the two amplifier inputs will result in a smaller error than either bias current alone would produce.

11. ***Input offset voltage: $V_{OS}$***
$V_{OS}$ is the voltage required at the input of an amplifier to produce zero output. Most often this parameter is measured in the opposite manner, namely, the output voltage resulting from a zero input. With a given gain configuration the output voltage is divided by the noninverting gain of the circuit to determine the voltage at the input (referred to the input or RTI).



**12. *Input voltage noise: $V_N$***

$V_N$ is the noise component of voltage offset. The noise is measured at the output with a true RMS meter and referred to the input. Low pass and bandpass filters may be used to limit meter response. At any given −3db bandwith, the RMS value is divided by the square root of that bandwidth to obtain the spectral noise density.

**13. *Input current noise: $I_N$***

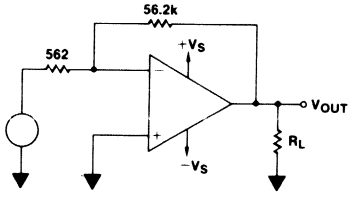
$I_N$ is the noise component of bias current. It is an RTI specification similar to current offset. The use of the filters and the calculation of spectral noise density is similar to the procedures used for voltage noise.

**14. *Power supply rejection: PSR***

PSR is the ability of the amplifier to reject the effect of changes in total supply voltage on voltage offset. Dual supplies are varied simultaneously to test this parameter. Supply values will include the minimum and maximum operating specifications. Changing from dual 15V supplies to dual 20V supplies is a 10V change of total supply voltage. A resulting 1mV offset change would indicate a PSR of 100$\mu$V/V or 80db. When PSR is plotted versus frequency, one supply at a time has the AC waveform impressed upon it.

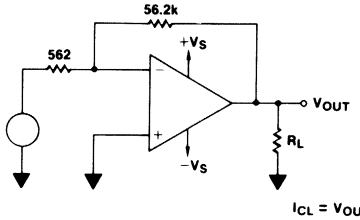
**15. *Output voltage swing: $V_O$***

$V_O$ is the minimum voltage swing capability of the amplifier and is usually specified at multiple current ratings. The amplifier is driven in excess of the specified output and then checked for minimum output with the appropriate load.




**16. *Current limit: $I_{CL}$***

With the amplifier overdriven, a small resistor is used to detect the point of current limiting. Resistance values and power supply voltages are selected to insure that a nonlimiting amplifier will be detected without excessive internal power dissipation.




$I_{CL} = V_{OUT}/R_L$

**17. *Slew rate: SR***

SR is the maximum rate of change of the output voltage. An inverting gain circuit is usually used with an input signal at least 10 times faster than the amplifier rating. Measurement points are between 10 and 90% of total output swing. Over driving the amplifier is permissible though at times may result in overload recovery problems.

**18. *Full power response:***

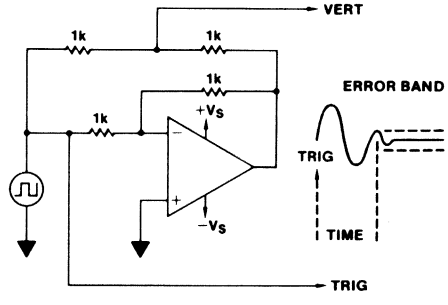
Full power response is the highest frequency at which the amplifier can drive a sine wave without visible distortion (3-5%) on an oscilloscope. Supply voltage is set to the typical rating. Power response curves relate the reduced output as a function of frequency but independent of gain.

**19. *Gain bandwidth product:***

Gain bandwidth product is the product of gain times frequency at a specified frequency. This is always measured at or below the unity gain frequency of the amplifier.

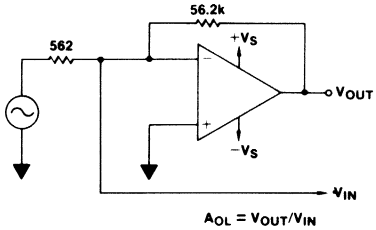
**20. *Settling time:***

Settling time is the time required for the amplifier to settle within a specified error of final value. Slewing time is included. This parameter is usually measured using the inverting gain of one circuit, a false summing junction, and a very fast rising input waveform triggering an oscilloscope.




**21. *Open loop gain: $A_{OL}$***

$A_{OL}$ is the actual gain from the inverting input pin to output, with the noninverting input grounded. If plotted versus frequency, it is called a bode plot.




$A_{OL} = V_{OUT}/V_{IN}$

$A_{OL}\ [db] = 20\ Log\ [V_{OUT}/V_{IN}]$

**22. *Open loop phase response:***

Open loop phase response is the actual phase from the noninverting input pin to output. While ideally between 0 and 90°, it may be higher. It is usually plotted versus frequency. Measurement techniques are similar to those used for open loop gain.

**23. *Phase margin:***

Phase margin is 180° less the open loop phase at the frequency where the open loop gain of the amplifier is unity.

**24. *Quiescent current: $I_Q$***

Quiescent current is the current drawn from each supply rail with zero output voltage and load current. (Insignificant differences between the two supply rail currents may exist due to input bias currents.)

# EQUIVALENT/SECOND SOURCES

This topic will be treated from two viewpoints: for the designer who knows the APEX part is ideal but must have a second source, and then for the designer using another part who must find a second source to improve performance, reduce cost or solve availability problems. If all specifications of a product were utilized to the fullest, this would be a very simple matter; all specifications must be equal. However, a design initiated before APEX developed its wide range of power op amps had very few options for high current applications. For example, if a hybrid FET input device was chosen, it may have had several properties not needed in the application. With today's choices, it is possible a bipolar input device may give superior performance or lower cost in the specific circuit.

***Due to the rapid development of power op amps, the second source question must be centered on the requirements of the application rather than specifications of the original component. The second source information is presented from this point of view.***

## APEX ALTERNATIVES FOR EXISTING DESIGNS . . .

**BURR-BROWN**

| | | |
|---|---|---|
| OPA501AM<br>OPA501BM<br>OPA501RM<br>OPA501SM | PA51[1]<br>PA51C[1]<br>PA51B[1]<br>PA51A[1] | Slightly improved thermal performance for all grades. Other specifications are identical. |
| | PA61[2] | Supplies to ±45V, drives closer to rails, offset currents are higher. |
| OPA511 | PA11[1] | Identical specifications but this part is not recommended for new designs. |
| | PA01[2] | Significant cost savings over OPA511 with only a slightly less performance. |
| | PA10[2] | Supplies to ±45V, improved voltage offset, faster, with only slightly higher cost. |
| OPA512BM<br>OPA512SM | PA12[1] | Specifications are essentially identical but thermisters in PA12 provide better control of quiescent current in high power/high temperature applications. |
| OPA8780 | | |
| UM | PA80Q[1] | Offers complete dynamic testing at −25/85°C. |
| VM | PA83-4[2] | Supplies to ±150V, also a non-mil part but with full dynamic testing at −55/125°C. |
| UM/883B | PA83M[2] | Supplies to ±150V with lower cost plus full dynamic testing. |
| VM/883B | PA83M[2] | Supplies to ±150V with lower cost plus full dynamic testing. |
| VM/MIL | PA83M[2] | We understand /MIL and /883 to be equivalent. |
| OPA8785 | | |
| UM | PA51Q[2] | 10A output test at 40% higher voltage. |
| VM | PA51A[1] | 10A output test at 30% higher voltage, commercial part, substantially lower cost. |
| UM/883V | PA51M[2] | 10A output test at 40% higher voltage, −55 to 125°C range, significant cost savings. |
| VM/883V | PA51M[2] | 10A output test at 30% higher voltage, voltage offset and drift about twice as great, *substantial* cost savings. |
| | PA61M[2] | Supplies to ±45V, drives closer to rails, offset currents are higher, *substantial* cost savings. |
| 3571, 72 | | All require: new current limits (position and value), external compensation not required. The 3572 is unique. If the circuit is converted, many models will fit the socket. Q versions are available. |
| | PA07[3] | Higher voltage, power dissipation, reliability and frequency response, high accuracy "A" and MIL-STD-883C "M" versions are available. |
| | PA01[3] | Bipolar input, supplies to ±28V, *very* cost effective when usable. |
| | PA10[3] | High performance bipolar input, supplies up to ±50V, substantially less expensive than 3572. |
| | PA12[3] | Output currents up to 15A, supplies up to ±50V, high performance bipolar input. |
| | PA51[3] | Output currents to 10A, bipolar input, class C output, is more cost effective than 3572. |

| | | |
|---|---|---|
| 3573 | PA73[1] | Specifications are identical, MIL-STD-883C "M" versions are available. |
| 3580-83 | PA83[2] | Extends the best specs of each model through the entire voltage range. |
| 3580J | PA80J[1] | All major specifications are identical. |
| 3580JQ | PA80Q[1] | All major specifications are identical. |
| 3581J | PA81J[1] | All major specifications are identical. |
| 3582J | PA82J[1] | All major specifications are identical. |
| 3582JQ | PA82Q[1] | All major specifications are identical. |
| 3583AM | PA83[1] | All major specifications are identical. |
| 3583AMQ | PA83Q[1] | All major specifications are identical. |
| 3583J | PA83J[1] | All major specifications are identical. |
| 3584JQ | PA84[1] | Slightly faster, improved phase margin, higher current, temperature range is −25 |
| 3584JMQ | PA84Q[1] | to 85°C on APEX parts instead of 0 to 70°C. |
| **INTERSIL** | | |
| 8510, 15, 20, 30 | PA01[4] | All APEX current models offer more power and several offer accuracy improvements. The models listed here are 5A, 67W devices. All are 8 pin TO-3 units but Intersil pin assignments are different. |
| | PA07[4] | |
| | PA10[4] | |
| | PA11[4] | |
| | PA73[4] | |
| **NATIONAL** | | |
| LH0101 | PA02[3] | The PA02 swing enhancement network is internal, PC layout can often accept either part, case is isolated, better speed and linearity, ±19V supplies maximum. |
| **TELEDYNE** | | |
| 1460 | PA09[4] | Faster and considerable more power. |
| 1461 | PA09[4] | Slower but more power, package totally different. |
| 1480 | PA83[4] | Similar performance. |
| | PA84[4] | Faster (external compensation), but less current output. |

# POSSIBLE SECOND SOURCES FOR APEX PRODUCTS . . .

**PA01** OPA511[2] Burr-Brown; Slightly better voltage swing and voltage offset but much more costly.

**PA02** LH0101[3] National; PC layout can be designed to accept either, output=case, may require external swing enhancement network, some loss of speed and linearity.

**PA03** None known.

**PA07** 3572[3] Burr-Brown; Reduced voltages and frequency, different current limits (position and value).

**PA08** None known.

**PA09** 1460[4] Teledyne; Bipolar input, .15A output.
1461[4] Teledyne; Faster, .6A output, DIP package.

**PA10** OPA511[2] Burr-Brown; Lower supply voltage, frequency, accuracy.
OPA512[2] Burr-Brown; 10A output, but higher cost.

**PA11** OPA511[1] Burr-Brown;

**PA12** OPA512[1] Burr-Brown;

**PA51** OPA501[1] Burr-Brown;

**PA61** None known.

**PA73** 3573[1] Burr-Brown;

**PA80J** 3580J[1] Burr-Brown;

**PA81J** 3581J[1] Burr-Brown;

**PA82J** 3582J[1] Burr-Brown;

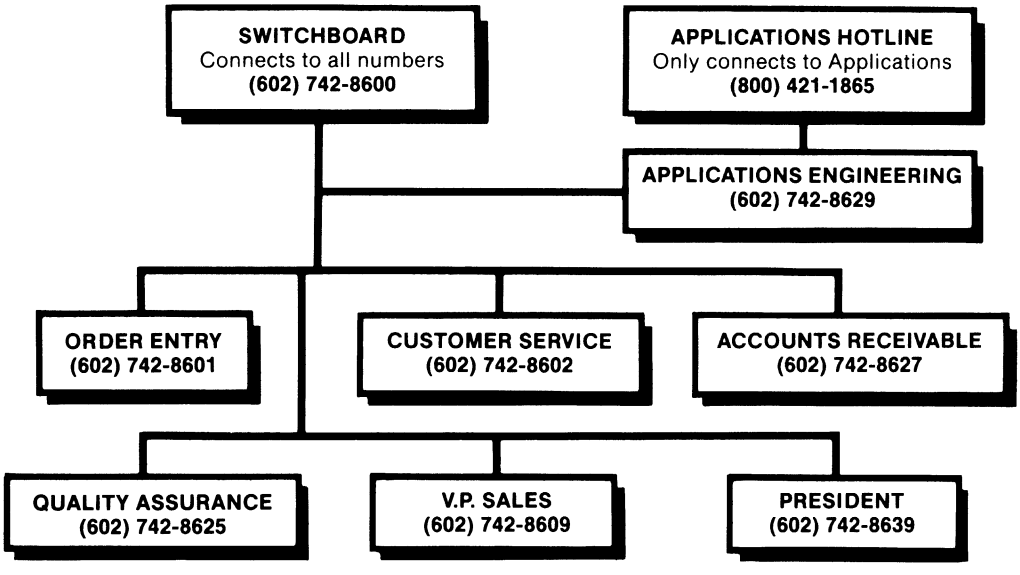
**PA83** 3583[2] Burr-Brown; Supplies down to ±50V only.

**PA84** 3584[2] Burr-Brown; Slightly slower, supplies down to ±70V only.

NOTES: (1) Form, fit and functional replacement. (2) A drop-in replacement — major performance differences are noted. (3) Functional replacement which may require minor circuit modifications. (4) Devices are similar — consult both data sheets to determine compatibility in your application. (5) Price comparisons made using catalog data published in 1985.

# ACCESS DIRECTORY

## TELEX: 170631




## STANDARD HOURS:

| | MOUNTAIN STANDARD TIME | GREENWICH MEAN TIME |
|---|---|---|
| SWITCH BOARD: | 8:00 AM to 4:30 PM | 15:00 to 23:30 |
| ORDER ENTRY: | 7:00 AM to 5:00 PM | 14:00 to 24:00 |
| OTHER: | 8:00 AM to 4:00 PM | 15:00 to 23:00 |

**APEX MICROTECHNOLOGY CORP. (Domestic)**
**APEX F.S.C. INC. (Export)**
5980 N. SHANNON ROAD, TUCSON, AZ 85741, USA

# NOTES

# APEX µtech ORDERING • TERMS • CONDITIONS

**POWER OP AMPS & ACCESSORIES • MADE IN USA**

## TO ORDER CALL (602) 742-8601

### HOW TO ORDER

**APEX MICROTECHNOLOGY** ships most small orders from stock. If you need immediate delivery, call us direct before 10 AM MST and specify "EXPRESS" service. We will make every effort to ship on the same day via Federal Express Overnight Service. Orders for five or more amplifiers are normally scheduled for delivery according to customer requirements and our work in process at APEX.

### EXPORT ORDERS

**APEX F.S.C.**, the export arm of APEX MICROTECHNOLOGY is represented throughout the industrialized free world by exclusive distributors who offer technical assistance and/or data sheets as well as speedy delivery at commpetitive prices. Please place your orders with the distributor in your country. For a list of distributors, see the back cover of this Handbook. Evaluation orders can be shipped without delay to most countries. However, most orders over U.S. $500.00 require a U.S. export license and in some cases an immport certificate from your government. Please allow 4-6 weeks for processing of these documents.

## TERMS AND CONDITIONS

**SHIPMENTS** will be fully insured and sent via UPS in the Southwest and UPS-Blue to all other locations unless otherwise specified. F.O.B. is Tucson, AZ. For shipments via the Postal Service a $6.00 surcharge will be added to the invoice.

**MINIMUM ORDER** is U.S. $30. — plus shipping and applicable taxes.

**LOST OR DAMAGED SHIPMENT** Contact the Common Carrier and APEX at once. Failure to do so within 30 days from shipment date will void the insurance claim. APEX MICROTECHNOLOGY is not responsible for loss or damage in transit, but will process the insurance claim for you. If the shipment was required to be uninsured, APEX will supply proof of shipment, thereby creating a legal obligation to pay the original invoice when due.

**PRODUCT RETURNS** within 30 days of shipment, will be accepted only if prior authorization has been obtained from APEX and the units have been used within the specified operating conditions. No solder residue should be found on the pins. Restocking charges are: 25% for standard industrial products. Custom and military products are not returnable.

**PRICES** are published in the latest U.S. price list. F.O.B. is Tucson, AZ U.S.A. Applicable state and local taxes will be added.

**CANCELLATION CHARGES** are 15% for standard products. For customized products they are:
- 25% if components purchase orders have been placed.
- 50% if parts assembly has been started.
- 75% if parts have been capped.

**PAYMENT TERMS** for approved accounts are net 30 days from the date of shipment, C.O.D. for new accounts without D & B rating. Past due accounts will be charged a .06% per day late fee.

**BILLING** in duplicate is done on the day of shipment. Federal Express or other airfreight charges will be billed by the carrier directly to the customer. On prepaid orders, the UPS shipping charges are paid by APEX.

**EXPORTS** may require a valid export license.

**APEX LIABILITY** is limited to replacement of product.

**EVALUATION** orders are available in the United States. Your purchase order must specify "Evaluation" and is limited to a quantity of two amplifiers and two mating sockets. If the amplifiers do not meet your needs, have not been damaged (used within specification), have not been soldered and are returned to APEX within 30 days, credit will be issued for both amplifiers and sockets.

## SERVICE

### APPLICATIONS HOTLINE (800) 421-1865

Unequaled technical support is available via the APEX MICROTECHNOLOGY Applications Hotline. A top notch engineer with previous design experience will help you select the most cost effective product for your application or will suggest the best circuit.

### WARRANTY

All products manufactured and sold by APEX MICROTECHNOLOGY are warranted to be free of defects under specified operating conditions for a period of 2 years from the original shipment date. Conformance to specifications at time of shipment is certified.

The warranty applies only to the original customer and is in lieu of all other warranties, expressed or implied. Under no condition will APEX MICROTECHNOLOGY be liable for any anticipated profits, consquential damages, loss of time or other losses incurred by the customer in connection with the purchase and/or use of the product.

### QUALITY ASSURANCE

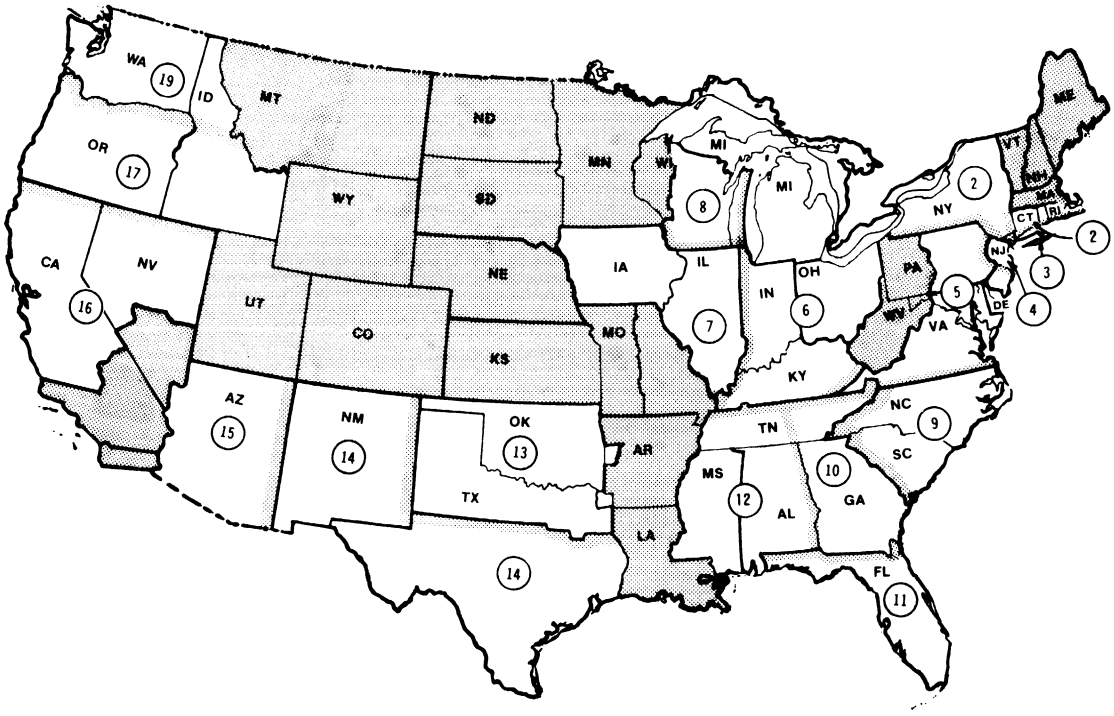
All APEX MICROTECHNOLOGY industrial grade products are functionally tested and visually inspected to the intent of method 2017.1 (excluding 2010.3) of MIL-STD-883C prior to capping. After the package is hermetically sealed, all guaranteed electrical parameters are tested 100%. Final marking includes a date/lot code fully traceable to the flow sheets kept on record. Quality assurance reports directly to the president of the company.

### FAILURE ANALYSIS

In case of failure within the warranty period, DO NOT RETURN the product without first contacting the APEX Customer Service Department to explain the problem and receive shipping instructions.

The device will be tested opened and inspected visually to determine the cause of failure. This information will help you maximize reliability and avoid future failures. A "Failure Analysis" will be supplied free of charge.

# U.S. SALES REPRESENTATIVES

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| 11 | Orlando, FL | Currie, Peak & Frazier, Inc. | Walt Currie | (305) 855-0843 |
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| 16 | Los Altos, CA | Kolm Marketing Assoc. | Henry Kolm | (415) 948-2635 |
| 17 | Beaverton, OR | Quest Marketing | Charles de Turene | (503) 641-7377 |
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☒ States without representation please call the APEX Microtechnology Sales Department.

# INDEX

## General Information



## Power Op Amp Models



## Applications Information